

L64500

MIL-STD-1750A

Microprocessor

Preliminary

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Description

The LSI Logic L64500 is a monolithic 1.5-micron drawn (0.9-effective) HCMOS chip which implements the MIL-STD-1750A (Notice 1) Instruction Set Architecture (ISA). The L64500 is a 16-bit Central Processing Unit (CPU) used for real-time processing. The CPU uses a sophisticated ALU architecture which is expandable up to 32 bits depending on the operation. The L64500 uses separate address and data buses to improve system performance and has advanced look-ahead capability with the optional L64550 (MBU) to minimize the probability of wait-state insertion.

The L64500 can be augmented with an L64550 (MBU) chip to implement optional enhancements of the MIL-STD-1750A. The L64550 includes the Memory Management Unit (MMU) with memory expansion capabilities up to 1M words of memory, the Block Protect Unit (BPU), Memory Fault Status Register

(MFSR), the Bus Arbitration Unit (BAU) with six bus masters, Start-up ROM interface, Discrete I/O Port, Trigger-go Counter and other options.

The L64500 CPU and the L64550 MBU chips were designed as a system to optimize the performance.

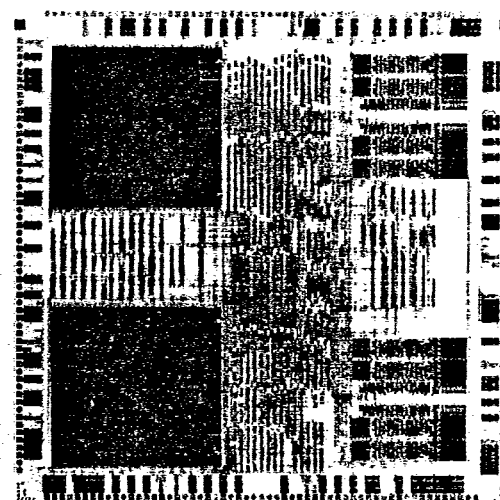
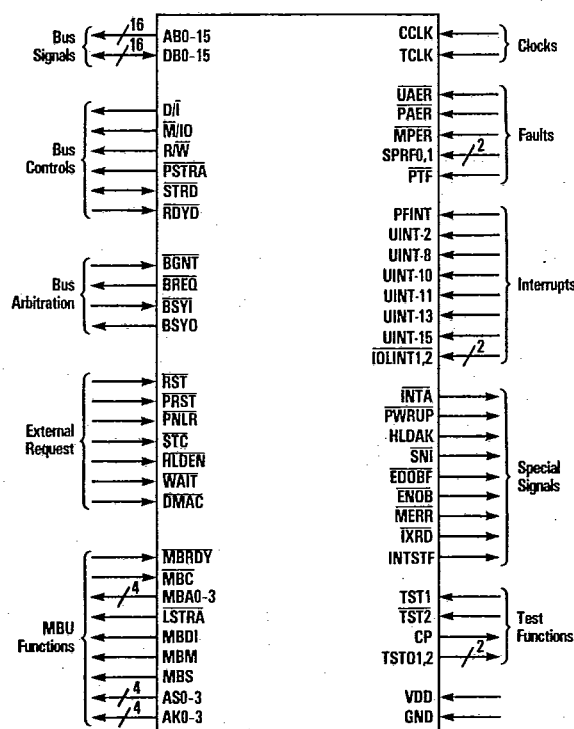
The L64500 and L64550 are included in LDS[®], LSI Logic's Design System, as ASIC library elements. These elements can be used as Gigacells[™] when combined with gate arrays or standard cells, or they can be used in multi-chip system simulations when adding new ASIC chips to the system.

The L64500 is available in several speed grades from 15 MHz to 25 MHz over the full military temperature range of -55°C to 125°C.

Features

- Single-chip high performance microprocessor
- Implements MIL-STD-1750A (Notice 1) Instruction Set
- 1.5-micron drawn (0.9-effective) HCMOS 2-layer metal cell-based technology
- 25 MHz operation over full military range
- Power dissipation ≤ 1 W
- TTL compatible interface
- Flexible packaging capability
- Available as ASIC Gigacell library element
- Performance optimized architecture
 - Split data and address bus
 - Variable width ALU: up to 32 bits
 - Instruction pre-fetch
 - Multiport register files
- Timers A and B option on-chip
- 64K word address space expandable to 1M word with optional MBU chip

Logic Symbol and Chip Layout



Chip Layout

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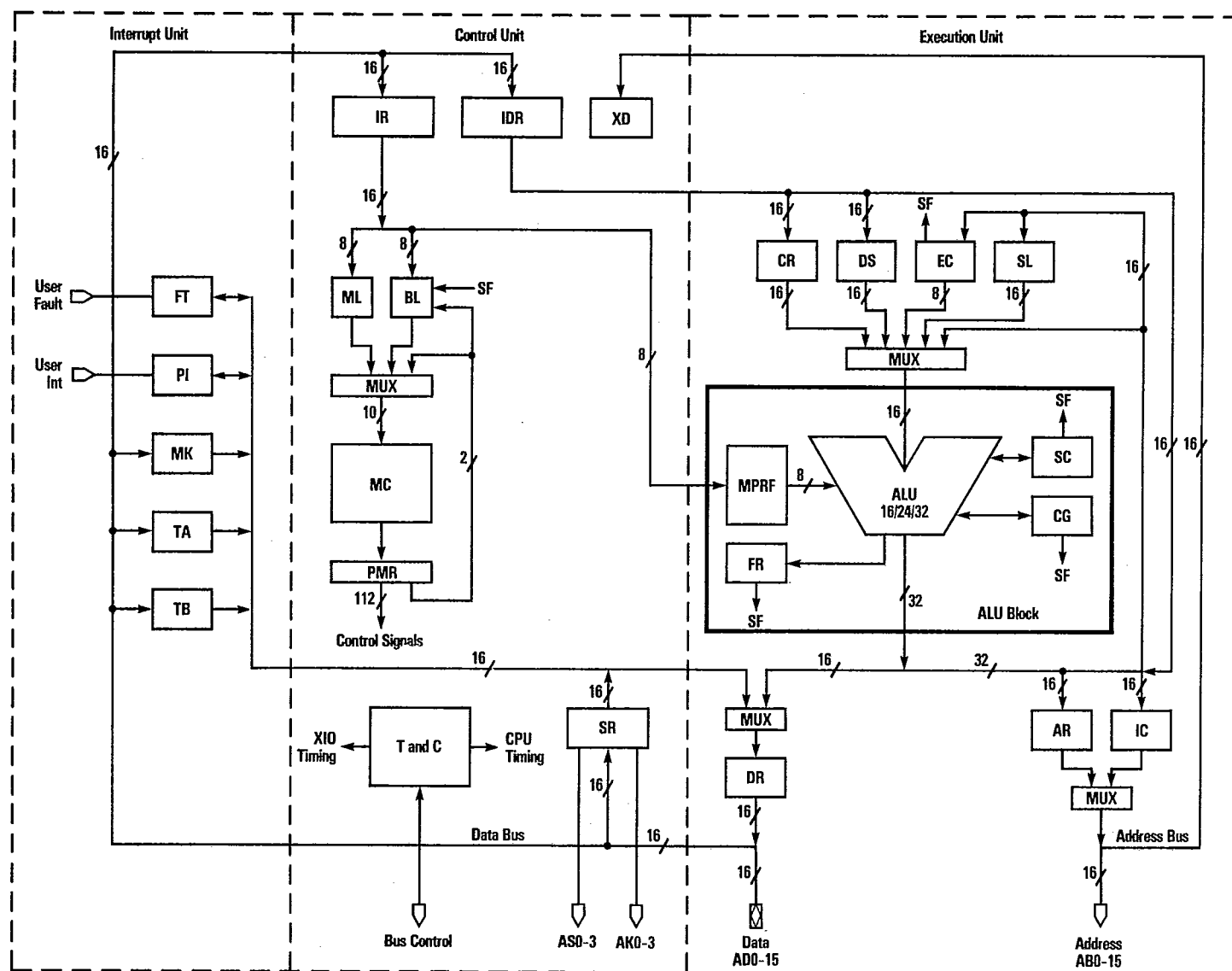
Architecture

The LSI Logic L64500 CPU is a high performance implementation of the MIL-STD-1750A (Notice 1) Instruction Set Architecture. It consists of a 128K-bit ROM, a 32-bit core ALU, and associated registers and controlling logic. The architecture has been designed for optimal performance. A key feature is a variable width ALU; 16, 24, and 32-bit words. In addition, the Address and Data buses have been separated to further increase performance.

The L64500 CPU can access a standard 64K word address space. With the optional L64550 MBU chip, the Memory Management Unit (MMU) can expand the address space up to one megaword.

In addition to implementing all of the required MIL-STD-1750A instruction set, the L64500 contains the optional Input/Output Interrupts and interval timers A and B. Other options such as Memory Fault Status Registers, Start-Up ROM interface, Trigger-go Counter and discrete I/O port are incorporated in the optional L64550 MBU chip.

The L64500 (CPU) and L64550 (MBU) were designed as a system to minimize timing issues between the chips. There are special carry lookahead features built in to the chips to maintain system performance. System performance will not decrease with the addition of the L64550 (MBU).

**L64500 CPU Block Diagram**

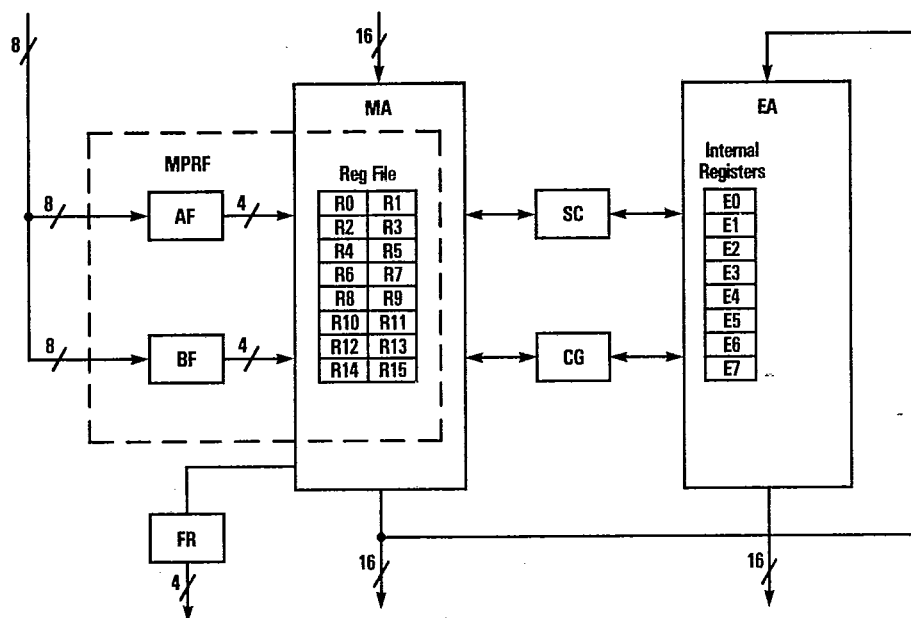
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ALU Block: ALU and Register File Organization

Block Description

AF: Main ALU, A-Port Register File Address
 ALU: Arithmetic/Logic Unit
 AR: Address Register
 BF: Main ALU, B-Port Register File Address
 BL: Branch Logic
 CG: Carry Generate
 CR: Constant ROM
 DR: Data Register
 DS: Data Swap
 EA: Extended ALU
 EC: Event Counter
 FR: Flag Register
 FT: Fault Register
 IC: Instruction Counter
 IDR: Input Data Register

IR: Instruction Register
 MA: Main ALU
 MC: Microcode ROM
 MK: Masking Register
 ML: Mapping Logic
 MPRF: Multi-Port Register File
 PI: Pending Interrupt and Priority Encoder
 PMR: Pipeline Micro Register
 SC: Shift Control
 SL: Shift Logic and Registers
 SR: Status Register
 T and C: Timing and Control
 TA: Timer A
 TB: Timer B
 XD: XIO Decode

Execution Unit

The Execution Unit provides the computational resources for the L64500. Key features include:

- Variable Width ALU
- Multiport Registers
- Constant ROM
- Data Swap Logic
- Event Counter
- Shift Logic

Main Arithmetic Logic Unit (MA)—The Main ALU consists of a high speed ALU with a 16-word by 16-bit 2-port RAM organized as R0..R15, and the associated shifting, decoding and multiplexing logic.

The Carry Generate (CG)—Generates a carry look-ahead signal for the ALUs.

Extended Arithmetic Logic Unit (EA)—The Extended ALU is architecturally the same as the MA but it contains only 8 registers (E0..E7). These 16×8 registers are used internally.

Shift Control (SC)—This logic controls all the linking operations when configuring the ALU into variable bit widths of 16, 24, and 32. The Main ALU and Extended ALU can be used in parallel allowing for substantial reduction of execution times.

A-Port and B-Port Register Files (AF, BF)—The MPRF block is comprised of the AF and BF registers. These registers generate and execute the address for the Main ALU register files R0 through R15.

Flag Register (FR)—This register saves the status of the current operation in the Main ALU.

Instruction Counter (IC)—The counter holds the address of the next instruction to be executed.

Address Register (AR)—This register contains the next address for the data operands.

Data Register (DR)—This register holds the current data. During the write cycle, this register will be transparent.

Constant ROM (CR)—A 512 word by 16 bits/word ROM which holds constant data and address locations that require fast access.

Data Swap (DS)—Used by ALU to swap 8-bit data. Each 8-bit data swap is done on one clock cycle.

Event Counter (EC)—Multifunction 8-bit counter used by the ALU to count up/down during execution (as required).

Shift Logic (SL)—16-bit register used by ALU for shift operations.

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Control Unit

The microcode in the L64500 controls the execution of the major functional blocks.

Microcode ROM (MC)—A 1K (1024) word by 112 bits/word ROM which translates the MIL-STD-1750A Instruction set into microinstructions controlling the processor.

Pipeline Micro Register (PMR)—This register follows the Microcode ROM increasing the performance of the processor by fetching the next microinstruction during the current cycle.

Mapping Logic (ML)—A 1K-word by 8 bits/word ROM which stores MIL-STD-1750A opcode map vectors. These vectors translate opcodes into starting addresses for corresponding microcode sequences and are used by the microsequencer.

Timing and Control (T and C)—The L64500 utilizes a state machine, clocked by the system clock (CCLK), to generate processor timing and control signals. These signals constitute the lowest level of control available within the module and provide the framework for such basic operations as selecting the next microinstruction to be executed, sequencing bus control signals to effect a memory transfer, or performing an operation within the ALU. Each complete pass through the state machine corresponds to one such operation and constitutes a machine cycle.

A complete machine cycle requires four or more oscillator cycles with the exact number determined by the type of operation being performed. Internally decoded XIO commands and external processor operations require a minimum of five oscillator cycles to be completed.

The internal ready signal is generated by the Interrupt Unit whenever an internally decoded XIO command is detected. An external ready interface is provided which allows external machine cycles to be extended when interfacing with slow devices. The external ready signal is provided by external system logic and must be asserted in order to conclude the machine cycle.

Instruction Register (IR)—This register contains four multilevel 16-bit registers. These registers which are used to hold the next instruction to be executed, can be operated in different modes; a dual 2-level pipeline register and a single 4-level pipeline register.

Input Data Register (IDR)—This register contains four multilevel 16-bit registers. These registers which are used to hold operands, can be operated in different modes; a dual 2-level pipeline register and a single 4-level pipeline register.

Branch Logic (BL)—Contains the address of the next microinstruction and can terminate the current operations depending on the execution status flag from the event counter, or flag registers, or ALU.

Status Register (SR)—A 16-bit register which holds the condition status (CS) bits C, P, Z and N; the 4-bit address state (AS) field; and the 4-bit processor state (PS) files. The CS bits are updated after each logical, shift and arithmetic operation performed by the ALU. The Control Unit interrogates these bits during conditional operations to determine which course of action follows. The AS field is used during extended memory access to define the page register set to be used for instruction and operand memory references. The PS field is also used during execution of privileged instructions. PS must be zero for such operations to be legal. Figure 1 depicts the status word register format.

XIO Command Decode Logic (XD)—This logic decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action.

Field	Bits	Description
CS	0	Condition-Status C – Carry from an addition or no borrow from a subtraction
	1	P – Result > 0
	2	Z – Result = 0
	3	N – Result < 0
R	4 – 7	Reserved
PS	8 – 11	Processor State (a) – Memory access key code (b) – Privileged instruction indicator
AS	12 – 15	Address State Page register sets for expanded memory addressing

0	3 4	7 8	11 12	15
CS	R	PS	AS	

Figure 1. Status Word Format

Interrupt Unit

The Interrupt Unit incorporates a pending interrupt register and priority encoder (PI), a mask register (MK), a fault register (FT), two interval timers (A and B) and XIO command decode logic. A brief description of these features follows:

Pending Interrupt (PI)—This block contains the pending interrupt register and priority encoder. The pending interrupt register is a 16-bit register used to capture and hold interrupts. PI supports three dedicated external, six user-definable external and seven dedicated internal interrupts as defined by MIL-STD-1750A. Power Fail (PFINT) and User Interrupts (UINT) are captured on the HIGH-to-LOW transition. I/O level interrupts are level sensitive. Figure 2 defines PI bit assignment. The priority encoder generates an interrupt request to the Control Unit whenever one or more unmasked interrupts are pending in pending interrupt register (PI) and encodes the highest priority unmasked pending interrupt as a 4-bit vector. This vector is read by the Execution Unit during interrupt servicing to create the interrupt linkage and service pointers.

Mask Register (MK)—This 16-bit register is used to store the interrupt mask. Interrupts are masked by

"ANDing" each mask bit with its counterpart PI register bit. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level 0 (PFINT) can not be masked. A LOW in a given bit position indicates that the corresponding bit in the PI register will be masked.

Fault Register (FT)—This 16-bit register is used to capture and hold both internal and user implemented external faults. Setting any one or more faults in FT will cause a logic HIGH (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command. Figure 3 defines FT bit assignments.

Timers A and B (TA, TB)—Two 16-bit software controllable timers. Timer A is clocked by the TCLK (100 KHz as defined in MIL-STD-1750A) input while timer B is clocked by the internally generated 10 KHz clock. Timers A and B will generate interrupt levels 7 and 9, respectively (Figure 2) when their maximum counts of 65,536 are reached. (Timers A and B can be disabled by applying a LOW to pin STC.)

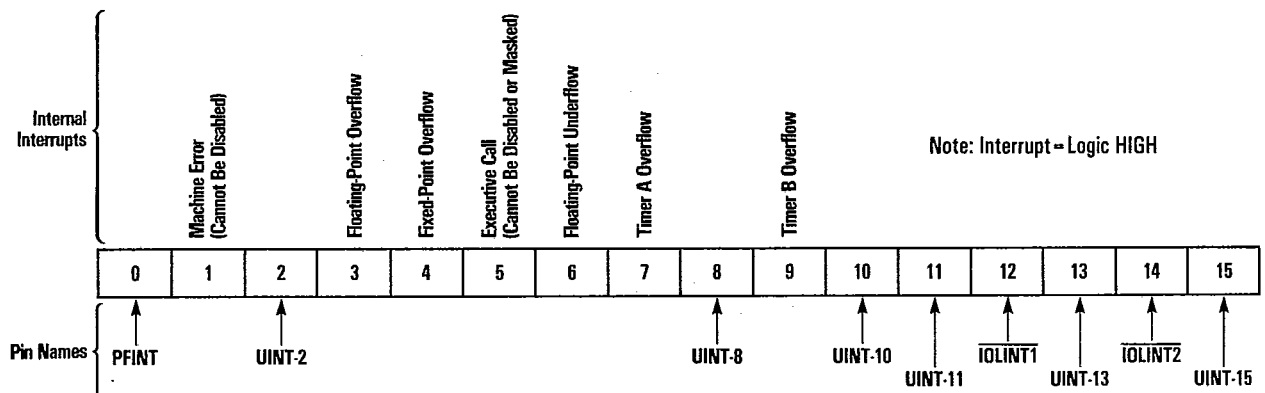


Figure 2. Pending Interrupt Register Bit Assignments

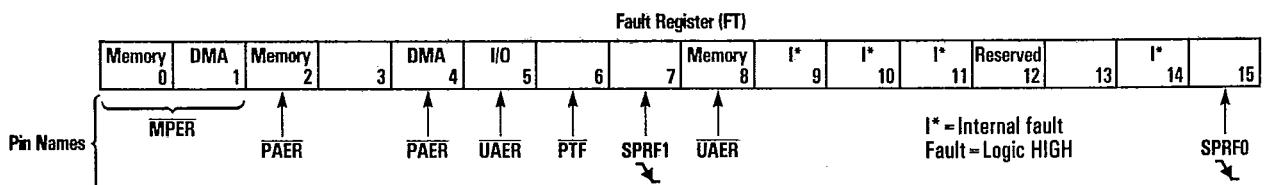


Figure 3. Fault Register Bit Assignments

Pin Descriptions

The logic symbol on the front page of this data sheet defines the different pin groupings outlined in this section. The pin groupings are: Bus Signals, Bus Controls, Bus Arbitration, External Request, MBU Functions, Clocks, Faults, Interrupts, Special Signals and Test Functions. Figure 4 defines the pin assignments for the L64500. All inputs and outputs are TTL compatible; see DC table for complete information. All I/Os are protected against latch-up and static discharge to a specification of 200 mA and 2000 V respectively.

Pin descriptions follow, split out by functional groupings.

Power and Ground (VDD, VSS)—There are 26 VDD and VSS pins to distribute the power and ground requirements of the chip. These additional pins will reduce noise due to typically high transient currents generated by fast switching HCMOS output drivers. Standard TTL voltage levels can be applied (see DC specifications).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	TCLK	TST2	TST01	DB2	DB3	DB4	DB6	DB7	DB9	VDD	DB12	DB15	NC
B	NC	NC	VDD	STC	TST02	DB0	DB1	DB5	DB8	DB10	VSS	DB14	NC	VSS	AB13
C	AK2	VDD	NC	NC	VSS	VSS	VDD	VSS	VSS	DB11	DB13	NC	AB15	AB12	AB11
D	VSS	AK0	NC										AB14	VDD	AB10
E	AS2	AK3	AK1										VSS	AB9	AB8
F	VDD	AS1	AS0										NC	AB7	AB5
G	MBS	AS3	VSS										VSS	AB6	AB4
H	INTA	IXRD	INTSTF										VDD	AB2	AB3
J	UINT-2	UINT-10	PFINT										VSS	MBA3	AB1
K	UINT-8	VSS	UINT-11										MBA0	MBA1	AB0
L	IOLINT1	UINT-13	NC										SPRF10	VDD	MBA2
M	IOLINT2	VDD	R/W										NC	PTF	VSS
N	UINT-15	TST1	M/I/O	NC	NC	BSYI	VSS	ED0BF	ENOB	HLDK	PNLR	UAER	MPER	NC	SPRF1
P	MBC	NC	D/I	MBDI	RDYD	BGMT	BSYO	LSTRA	SNI	CP	VSS	HLDEN	DMAC	NC	PAER
Q	NC	MBM	WAIT	MBRDY	BREQ	VDD	PSTRA	STRD	VSS	CCLK	PWRUP	PRST	RST	MERR	NC

Figure 4. L64500 Pin Diagram (Top View)

Pin Descriptions
(Continued)

Name	Symbol	Pin	Description
BUS SIGNALS			
Address Bus	AB15 AB14 AB13 AB12 AB11 AB10 AB9 AB8 AB7 AB6 AB5 AB4 AB3 AB2 AB1 AB0	C13 D13 B15 C14 C15 D15 E14 E15 F14 G14 F15 G15 H15 H14 J15 K15	Outputs used to indicate the memory address or I/O location. AB0 is the most significant bit (MSB). These lines are 3-state during bus cycles not assigned to the CPU.
Data Bus	DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	A14 B12 C11 A13 C10 B10 A11 B9 A10 A9 B8 A8 A7 A6 B7 B6	A 16-bit bidirectional data bus used to transmit or receive data from the memory or I/O location. DB0 is the most significant bit (MSB). These lines are 3-state during bus cycles not assigned to the CPU.
BUS CONTROL			
Data or Instruction	D/I	P3	An output signal that indicates whether the current bus cycle access is for Data (HIGH) or for Instruction (LOW). This signal is 3-state during bus cycles not assigned to the CPU.
Memory or I/O	M/I/O	N3	An output signal that indicates whether the current bus cycle is for Memory (LOW) or I/O (HIGH). This signal is 3-state during bus cycles not assigned to the CPU.
Read or Write	R/W	M3	An output signal that indicates whether the current bus cycle is a Read (HIGH) or Write (LOW). This signal is 3-state during bus cycles not assigned to the CPU.
Physical Strobe Address	PSTRA	Q7	An active LOW output that can be used to externally latch the memory or XIO address at the LOW-to-HIGH transition of the strobe. This signal is 3-state during bus cycles not assigned to the CPU.
Strobe Data	STRD	Q8	A bidirectional signal. When the output signal is LOW, it can be used to strobe data during the memory or XIO cycles. During bus cycles not assigned to the CPU (output disabled), the trailing edge of the input signal (LOW-to-HIGH) is used for sampling bits into the Fault Register. NOTE: This pin should never float.
Ready Data	RDYD	P5	An active LOW input usually asserted by memory or the I/O device to indicate the completion of a Data cycle. When RDYD is not active, Wait states are inserted by the CPU. This will stretch out the bus cycle until RDYD is active.

Pin Descriptions
(Continued)

Name	Symbol	Pin	Description
BUS ARBITRATION			
Bus Grant	$\overline{\text{BGNT}}$	P6	An active LOW input from an external arbiter that indicates the CPU may use the bus.
Bus Request	$\overline{\text{BREQ}}$	Q5	An active LOW output indicates the CPU is ready to execute a bus cycle. During internal CPU cycles this output is inactive (HIGH).
Busy In	$\overline{\text{BSYI}}$	N6	An active LOW input indicates to the CPU that the bus is currently in use.
Busy Out	$\overline{\text{BSYO}}$	P7	An active HIGH output indicates that the CPU is currently using the bus. NOTE: During the execution of the TSB instruction, the bus will remain "locked" until the completion of the instruction. The BSYO signal will remain HIGH until the completion of the instruction.
CLOCK			
CPU Clock	CCLK	Q10	Input clock signal (square wave, 40% to 60% duty cycle)
Timer Clock	TCLK	A3	A 100 KHz square wave clock input used for timers A and B.
EXTERNAL REQUEST			
Reset	$\overline{\text{RST}}$	Q13	A synchronous active LOW input that initializes the CPU in accordance to MIL-STD-1750A. The initialization is executed after the completion of the current internal CPU cycle.
Panel Request	$\overline{\text{PNLR}}$	N11	An active LOW input that causes the CPU to HALT and to enter into the Panel mode allowing the user to perform Panel operations.
Power Up Reset	$\overline{\text{PRST}}$	Q12	An asynchronous active LOW input that initializes the CPU in accordance to MIL-STD-1750A. This signal should be used during the power-up sequence.
Stop Counters	$\overline{\text{STC}}$	B4	An active LOW input that inhibits the counting of timers A and B.
Hold Enable	$\overline{\text{HLDEN}}$	P12	An active LOW input that enables the CPU to respond to the $\overline{\text{PNLR}}$ input. NOTE: If $\overline{\text{HLDEN}}$ is LOW, the BPT instruction will place the CPU in HALT mode allowing for Panel operations. When $\overline{\text{HLDEN}}$ is HIGH, the BPT instruction is treated as a NOP.
Wait	$\overline{\text{WAIT}}$	Q3	An active LOW input extends the bus cycle.
DMA Cycle	$\overline{\text{DMAC}}$	P13	An active LOW input asserted by an external bus arbiter indicating that the bus is currently granted to the DMA device. This signal is used by the CPU to enable the sampling of the DMA faults.
FAULTS			
Unimplemented Address Error	$\overline{\text{UAER}}$	N12	An active LOW input sampled by the Fault Register at the end of each bus cycle asserted by the CPU. If $\overline{\text{UAER}}$ is LOW during the memory cycle, bit 8 is set. If it is LOW during the I/O cycle, bit 5 is set.
Parity Error	$\overline{\text{PAER}}$	P15	An active LOW input sampled by the Fault Register. If $\overline{\text{PAER}}$ is LOW during the memory cycle, bit 2 is set. In the DMA cycle ($\overline{\text{DMAC}}$ is LOW), the $\overline{\text{PAER}}$ is sampled by the $\overline{\text{STRD}}$ signal and bit 4 is set.
Memory Protect Error	$\overline{\text{MPER}}$	N13	An active LOW input sampled by the Fault Register. If LOW during the memory cycle asserted by the CPU, bit 0 is set at the end of CPU cycle. In DMA cycle ($\overline{\text{DMAC}}$ is LOW), $\overline{\text{MPER}}$ is sampled by the $\overline{\text{STRD}}$ signal and bit 1 is set. NOTE: This input is generated by the MMU or BPU of the L64500 MBU chip to indicate that an access fault, execute protect or write-protect violation has been detected.

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Pin Descriptions
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Name	Symbol	Pin	Description
FAULTS			
Spare Faults	SPRF0 SPRF1	L13 N15	These signals are asynchronous fault inputs that are active on the HIGH-to-LOW transition. When active, bit 15 (Pin L13) or 7 (Pin N15) of the Fault Register is set.
PID Transmission	PTF	M14	An active LOW input sampled by the Fault Register at the end of each bus cycle asserted by the CPU. When active LOW, bit 6 is set.
INTERRUPTS			
Power Fail Interrupt	PFINT	J3	This input is active on the HIGH-to-LOW transition and corresponds to the highest level priority interrupt.
User Interrupts	UINT-2 UINT-8 UINT-10 UINT-11 UINT-13 UINT-15	J1 K1 J2 K3 L2 N1	Six input signals that are active on the HIGH-to-LOW transition. The six interrupt signals correspond to the priority levels 2, 8, 10, 11, 13 and 15 as specified in MIL-STD-1750A.
I/O Levels	IOLINT1 IOLINT2	L1 M1	Two active LOW signals which correspond to interrupt priority levels 12 and 14 as specified in MIL-STD-1750A. NOTE: These inputs are level interrupts and should be removed with the INTA signal.
SPECIAL SIGNALS			
Hold Acknowledge	HLDACK	N10	An active HIGH output indicates the CPU is in PANEL HOLD mode. The CPU enters this mode only if the HLDEN input is LOW and the BPT instruction is fetched or if the HLDEN is LOW and the PNLN input was initiated.
Power Up	PWRUP	Q11	An active LOW output that is active when the CPU has successfully completed the built-in test during the initialization sequence.
Interrupt Acknowledge	INTA	H1	An active LOW output that occurs when an interrupt is serviced by the CPU. This output may be used in conjunction with the appropriate data bit to reset the acknowledged interrupt.
Start New Instructions	SNI	P9	An active LOW output that indicates a new instruction will start executing in the next cycle. This is useful for instruction tracing.
Enable Data Output Buffer	EDOB $\overline{F}$	N8	An active LOW output that indicates the direction of the data lines; out. This signal could be used to enable an external output buffer to the bus system.
Enable Output Buffer	ENOB	N9	An active LOW output that is used to enable an external output buffer for the address lines and bus controls.
Machine Error	MERR	Q14	An active LOW output indicating an error in the Fault Register.
Internal XIO Ready	IXRD	H2	An active LOW output indicating access to internally implemented XIO (i.e., MK, PIR, FT, Timers, etc.).
Interrupt Status Flag	INTSTF	H3	An output indicating the status of the interrupt mechanism. A HIGH indicates Enable and a LOW indicates Disable status. This signal is useful in the debugging phase of the user's software.

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Pin Descriptions
(Continued)

Name	Symbol	Pin	Description
MBU FUNCTION			
MBU Ready	MBRDY	Q4	An active LOW input from the MBU (L64550) chip. If the MBU is not used, this input should be connected to GND.
MBU Connected	MBC	P1	When the MBU (L64550) chip is used, this pin should be connected to GND. If it is not used, connect to VDD.
MBU Address	MBA3 MBA2 MBA1 MBA0	J14 L15 K14 K13	Four output signals used by the MBU (L64550) chip. If the MBU is not used, these signals should not be connected.
Logical Strobe Address	LSTRA	P8	An active LOW output used only by the MMU (in the MBU) to latch the logical memory address. If the MBU chip is not used, this signal should not be connected.
MBU Data or Instruction	MBDI	P4	An output signal used by the MBU (L64550) chip. If the MBU is not used, this signal should not be connected.
MBU Memory	MBM	Q2	An output signal used by the MBU (L64550) chip. If the MBU is not used, this signal should not be connected.
MBU Status	MBS	G1	An output signal used by the MBU (L64550) chip. If the MBU is not used, this signal should not be connected.
Address State	AS3 AS2 AS1 AS0	G2 E1 F2 F3	Four output signals used by the MBU (L64550) to select the Page Register in the MMU. These outputs are 3-state during bus cycles not assigned to the CPU.
Access Key	AK3 AK2 AK1 AK0	E2 C1 E3 D2	Four output signals used by the MBU (L64550) to match the Access Lock. These outputs are 3-state during bus cycles not assigned to the CPU.
TEST FUNCTION (Factory Use)			
Test 1	TST1	N2	This input is used for factory testing. This input must be connected to VDD.
Test 2	TST2	A4	This input is used for factory testing. This input must be connected to GND.
Clock Pulse	CP	P10	An output used for test purposes. On a LOW-to-HIGH transition, this input indicates the beginning of an internal CPU cycle. If RDYD is not activated or the WAIT signal is asserted, the LOW state of the CP signal is extended.
Test Outputs	TST01 TST02	A5 B5	These two inputs are for factory testing. USERS SHOULD NOT CONNECT THESE PINS.

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Timing Characteristics

This section gives timing characteristics for the L64500. Figures 5 through 9 depict the timing waveforms associated with L64500 signals including: Read Bus Cycle, Write Bus Cycle and Bus Access. Throughout these figures, the following abbreviated symbols are used:

Sn—Clock Cycles
 TL—HIGH-to-LOW Transition
 TH—LOW-to-HIGH Transition
 TS—Setup Time
 TD—Hold Time
 TZ—to High Impedance State
 TIS—Input Setup Time
 TOS—Output Setup Time

CPU Timing Characteristics (Preliminary): VDD=4.5V to 5.5V, TA = -55°C to 125°C, CL=50 pF

Pin Name	Symbol	Delay (ns)		
		Min	Typ	Max
BSY0	TL		12	19
	TH		10	16
	TD		15	24
M/I0, R/W, D/I	TS		20	32
	TD		22	35
PSTRA	TL		15	24
	TH		12	19
	TZ		15	24
AB0-15	TS		14	22
	TD		14	22
DB0-15	TIS		7	11
	TOS		20	32
	TD		5	8
STRD	TL		15	24
	TD		13	21
RDYD	TS		7	11
	TD		5	8
ENOB	TL		15	24
	TH		13	21
ED0BF	TL		15	24
	TH		13	21
BGNT	TS		7	11
	TD		5	8
BSYI	TS		7	11
	TD		5	8
BREQ	TL		20	32

Table 1

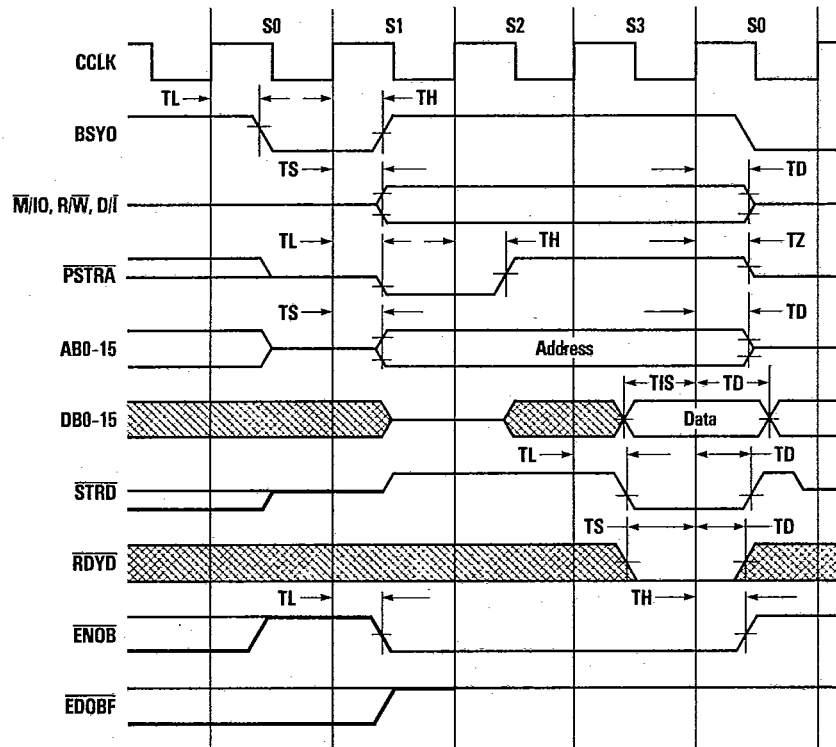


Figure 5. Minimum Read Bus Cycle

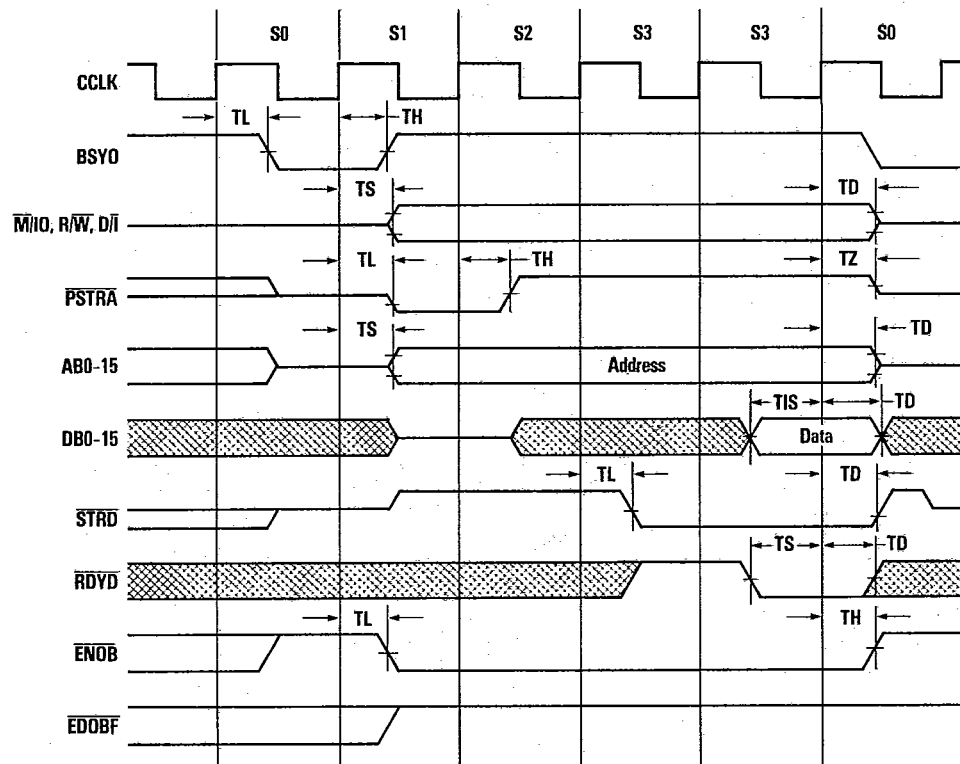


Figure 6. Extended Read Bus Cycle

L64500
MIL-STD-1750A
Microprocessor
Preliminary

5304804 L S I LOGIC CORP

90D 00975

D T-49-17-16

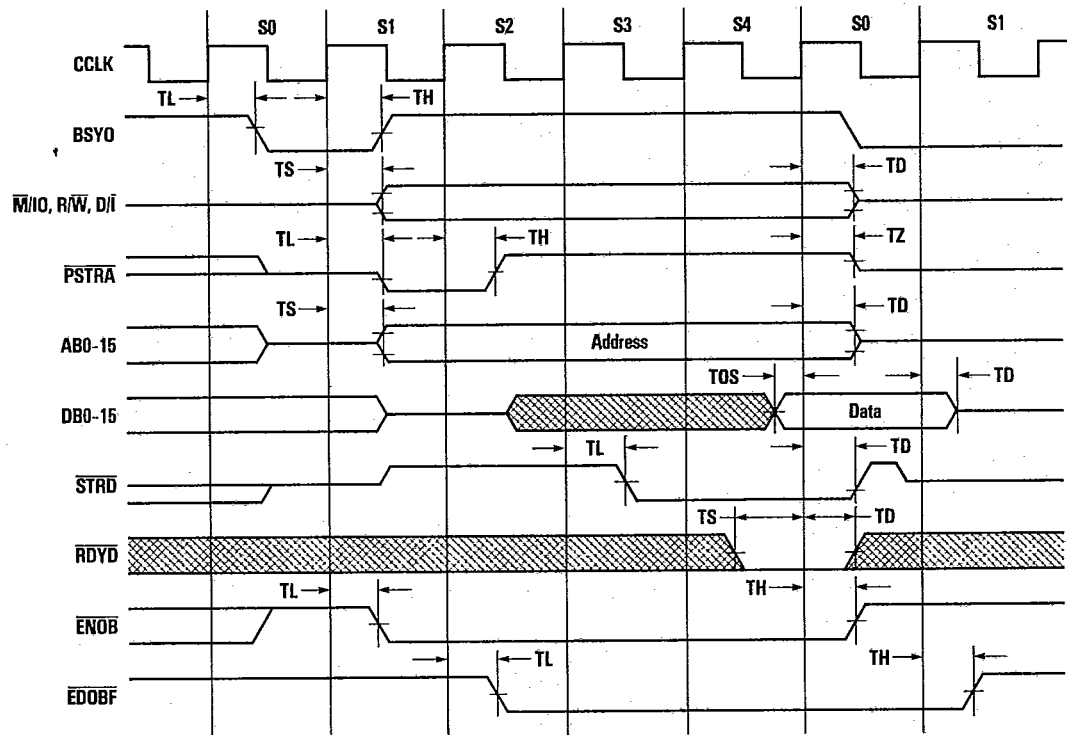


Figure 7. Minimum Write Bus Cycle

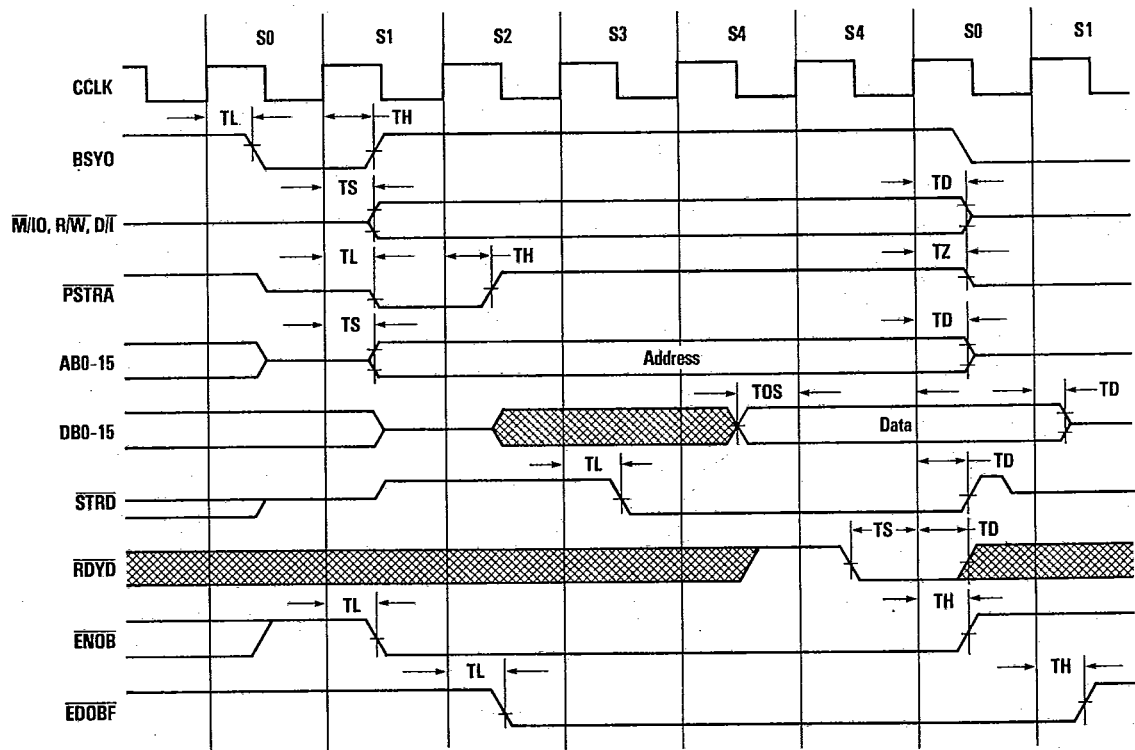


Figure 8. Extended Write Bus Cycle

L64500

MIL-STD-1750A

Microprocessor

Preliminary

LSI LOGIC

LSI LOGIC CORP 90 DE 5304804 0000976 1

5304804 L S I LOGIC CORP

90D 00976

D T-49-17-16

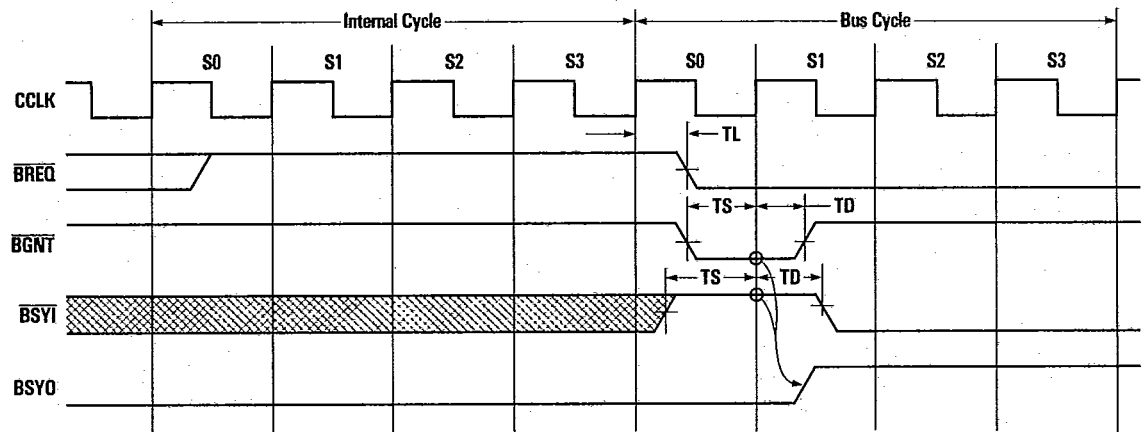


Figure 9. CPU Requirements for Accessing the Bus

L64500
MIL-STD-1750A
Microprocessor
Preliminary

LSI LOGIC

L S I LOGIC CORP 90 DE 5304804 0000977 3

5304804 L S I LOGIC CORP

90D 00977 D T-49-17-16

Instruction Summary

The following summary defines a number of the MIL-STD-1750A instructions and associated clock cycles.

To determine execution times multiply the clock cycle times with the clock cycle in nanoseconds (ns).

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments
LOAD/STORE								
Single-Precision Load	LR	R	81	1	0/0	0/0	4	
	LB	B	00	1	1/0	0/0	13	
	LBX	BX	40	1	1/0	0/0	13	
	LISP	ISP	82	1	0/0	0/0	4	
	LISN	ISN	83	1	0/0	0/0	4	
	L	D,DX	80	2	1/0	0/0	12	
	LIM	IM,IMX	85	2	0/0	0/0	8	
	LI	I,IX	84	2	2/0	0/0	17	
Double-Precision Load	DLR	R	87	1	0/0	0/0	12	
	DLB	B	04	1	2/0	0/0	17	
	DLBX	BX	401	1	2/0	0/0	17	
	DL	D,DX	86	2	2/0	0/0	16	
	DLI	I,IX	88	2	3/0	0/0	21	
Single-Precision Store	STB	B	08	1	0/1	0/0	9	
	STBX	BX	402	1	0/1	0/0	9	
	ST	D,DX	90	2	0/1	0/0	13	
	STI	I,IX	94	2	1/1	0/0	17	
Store a Non-Negative Constant	STC	D,DX	91	2	0/1	0/0	13	
	STCI	I,IX	92	2	1/1	0/0	17	
Double-Precision Store	DSTB	B	0C	1	0/2	0/0	15	
	DSTX	BX	403	1	0/2	0/0	14	
	DST	D,DX	96	2	0/2	0/0	18	
	DSTI	I,IX	98	2	1/2	0/0	22	
Load Multiple Registers	LM	D,DX	89	2	2/0	0/0	16	Add 4 clocks for each register load
Store Multiple Registers	STM	D,DX	99	2	0/1	0/0	12	Add 5 clocks for each store
BYTE								
Load From Upper Byte	LUB	D,DX	8B	2	1/0	0/0	16	
	LUBI	I,IX	8D	2	2/0	0/0	21	
Load From Lower Byte	LLB	D,DX	8C	2	1/0	0/0	16	
	LLBI	I,IX	8E	2	2/0	0/0	21	
Store Into Upper Byte	STUB	D,DX	9B	2	1/1	0/0	17	
	SUBI	I,IX	9D	2	2/1	0/0	22	
Store Into Lower Byte	STLB	D,DX	9C	2	1/1	0/0	17	
	SLBI	I,IX	9E	2	2/1	0/0	22	
Exchange Bytes in Register	XBR	S	EC	1	0/0	0/0	8	
COMPARE								
Single-Precision Compare	CR	R	F1	1	0/0	0/0	10	
	CB	B	38	1	1/0	0/0	17	
	CBX	BX	40C	1	1/0	0/0	17	
	CISP	ISP	F2	1	0/0	0/0	10	
	CISN	ISN	F3	1	0/0	0/0	10	
	C	D,DX	F0	2	1/0	0/0	18	
	CIM	IM	4A0A	2	0/0	0/0	14	
	CBL	D,DX	F4	2	2/0	0/0	31	
Compare Between Limits				2	2/0	0/0	21	
				2	2/0	0/0	26	
								D02 < D01 RA < D01
Double-Precision Compare	DCR	R	F7	1	0/0	0/0	18	
	DC	D,DX	F6	2	2/0	0/0	22	

F - Number of instruction fetches
R/W - Number of operand reads/writes
I/O - Number of input/output operations
C - Number of clock cycles
MO - Floating point derived operand mantissa
EO - Floating point 8-bit two's complement derived operand exponent
MA - Floating point register accumulator mantissa
EA - Floating point 8-bit two's complement register accumulator exponent
DO - Derived operand

Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments
INTEGER ARITHMETIC								
Single-Precision Integer Add	AR	R	A1	1	0/0	0/0	4	
	AB	B	10	1	1/0	0/0	13	
	ABX	BX	404	1	1/0	0/0	13	
	AISP	ISP	A2	1	0/0	0/0	4	
	A	D,DX	A0	2	1/0	0/0	12	
	AIM	IM	4A01	2	0/0	0/0	8	
Increment Memory by a Positive Integer	INCM	D,DX	A3	2	1/1	0/0	17	
Single-Precision Absolute Value of Register	ABS	R	A4	1	0/0	0/0	9	
Double-Precision Absolute Value of Register	DABS	R	A5	1	0/0	0/0	12	
Double-Precision Integer Add	DAR	R	A7	1	0/0	0/0	12	
	DA	D,DX	A6	2	2/0	0/0	16	
Single-Precision Integer Subtract	SR	R	B1	1	0/0	0/0	4	
	SBB	B	14	1	1/0	0/0	13	
	SBBX	BX	405	1	1/0	0/0	13	
	SISP	ISP	B2	1	0/0	0/0	4	
	S	D,DX	B0	2	1/0	0/0	12	
	SIM	IM	4A02	2	0/0	0/0	8	
Decrement Memory by a Positive Integer	DECM	D,DX	B3	2	1/1	0/0	17	
Single-Precision Negate Register	NEG	R	B4	1	0/0	0/0	4	
Double-Precision Negate Register	DNEG	R	B5	1	0/0	0/0	12	
Double-Precision Integer Subtract	DSR	R	B7	1	0/0	0/0	12	
	DS	D,DX	B6	2	2/0	0/0	16	
Single-Precision Integer Multiply with 16-Bit Product	MSR	R	C1	1	0/0	0/0	107	
	MISP	ISP	C2	1	0/0	0/0	108	
	MISN	ISN	C3	1	0/0	0/0	108	
	MS	D,DX	C0	2	1/0	0/0	115	
	MSIM	IM	4A04	2	0/0	0/0	111	
Single-Precision Integer Multiply with 32-Bit Product	MR	R	C5	1	0/0	0/0	101	
	MB	B	18	1	1/0	0/0	105	
	MBX	BX	406	1	1/0	0/0	105	
	M	D,DX	C4	2	1/0	0/0	109	
	MIM	IM	4A03	2	0/0	0/0	105	
Double-Precision Integer Multiply	DMR	R	C7	2	0/0	0/0	209	
	DM	D,DX	C6	2	2/0	0/0	209	
Single-Precision Integer Divide with 16-bit Dividend	DVR	R	D1	1	0/0	0/0	220	
				1	0/0	0/0	34	Divisor = 0
				1	0/0	0/0	26	Dividend = 0
				1	0/0	0/0	220	
				1	0/0	0/0	34	Divisor = 0
				1	0/0	0/0	26	Dividend = 0
	DISP	ISP	D2	1	0/0	0/0	220	
				1	0/0	0/0	34	Divisor = 0
				1	0/0	0/0	26	Dividend = 0
				1	0/0	0/0	220	
				1	0/0	0/0	34	Divisor = 0
				1	0/0	0/0	26	Dividend = 0
	DV	D,DX	D0	2	1/0	0/0	224	
				2	1/0	0/0	38	Divisor = 0
				2	1/0	0/0	30	Dividend = 0
				2	0/0	0/0	220	
				2	0/0	0/0	34	Divisor = 0
				2	0/0	0/0	26	Dividend = 0
	DVIM	IM	4A06	2	0/0	0/0	220	
				2	0/0	0/0	34	Divisor = 0
				2	0/0	0/0	26	Dividend = 0

F – Number of instruction fetches
R/W – Number of operand reads/writes
I/O – Number of input/output operations
C – Number of clock cycles
MO – Floating point derived operand mantissa
EO – Floating point 8-bit two's complement derived operand exponent
MA – Floating point register accumulator mantissa
EA – Floating point 8-bit two's complement register accumulator exponent
DO – Derived operand

Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments	
INTEGER ARITHMETIC									
Single-Precision Integer Divide with 32-Bit Dividend	DR	R	D5	1	0/0	0/0	220	Divisor = 0 Dividend = 0	
				1	0/0	0/0	34		
				1	0/0	0/0	30		
				1	1/0	0/0	224		
	DB	B	10	1	1/0	0/0	38	Divisor = 0 Dividend = 0	
				1	1/0	0/0	34		
				1	1/0	0/0	224		
				1	1/0	0/0	38		
	DBX	BX	407	1	1/0	0/0	224	Divisor = 0 Dividend = 0	
				1	1/0	0/0	38		
				1	1/0	0/0	34		
				1	1/0	0/0	224		
D	D,DX	D4	2	1/0	0/0	224	Divisor = 0 Dividend = 0		
			2	1/0	0/0	38			
			2	1/0	0/0	34			
			2	1/0	0/0	220			
DIM	IM	4A05	2	0/0	0/0	220	Divisor = 0 Dividend = 0		
			2	0/0	0/0	34			
			2	0/0	0/0	30			
			2	0/0	0/0	30			
Double-Precision Integer Divide	DDR	R	D7	2	0/0	0/0	207	Divisor = 0	
				2	0/0	0/0	25		
				2	2/0	0/0	211		
				2	2/0	0/0	29		
JUMP/BRANCH									
Jump on Condition	JC	D,DX	70	2	0/0	0/0	8	} Not taken	
	JCI	I,IX	71	2	0/0	0/0	8		
	JC	D,DX	70	3	0/0	0/0	16		} Taken
	JCI	I,IX	71	3	1/0	0/0	21		
Jump to Subroutine	JS	D,DX	72	2	0/0	0/0	12		
Subtract One and Jump	SOJ	D,DX	73	2	0/0	0/0	9	Not taken	
	SOJ	D	73	3	0/0	0/0	14		} Taken
		DX	730F	3	0/0	0/0	17		
				3					
Branch Unconditionally	BR	ICR	74	2	0/0	0/0	13		
Branch if Equal to (Zero)	BEZ	ICR	75	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
Branch if Less than (Zero)	BLT	ICR	76	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
Branch to Executive	BEX	S	77	2	5/3	0/1	94		
Branch if Less than or Equal to (Zero)	BLE	ICR	78	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
Branch if Greater than (Zero)	BGT	ICR	79	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
Branch if Not Equal to (Zero)	BNZ	ICR	7A	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
Branch if Greater than or Equal to (Zero)	BGE	ICR	7B	1	0/0	0/0	10	Not taken	
				3	0/0	0/0	13	Taken	
SHIFT									
Shift Left Logical	SLL	R	60	1	0/0	0/0	8	} Add 4 clocks for every shift performed	
Shift Right Logical	SRL	R	61	1	0/0	0/0	8		
Shift Right Arithmetic	SRA	R	62	1	0/0	0/0	8		
Shift Left Cyclic	SLC	R	63	1	0/0	0/0	8		
Double Shift Left Logical	DSLL	R	65	1	0/0	0/0	16		
Double Shift Right Logical	DSRL	R	66	1	0/0	0/0	16		
Double Shift Right Arithmetic	DSRA	R	67	1	0/0	0/0	16		

F – Number of instruction fetches
R/W – Number of operand reads/writes
I/O – Number of input/output operations
C – Number of clock cycles
MO – Floating point derived operand mantissa
EO – Floating point 8-bit two's complement derived operand exponent
MA – Floating point register accumulator mantissa
EA – Floating point 8-bit two's complement register accumulator exponent
DO – Derived operand

Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments	
SHIFT									
Double Shift Left Cyclic	DSLC	R	68	1	0/0	0/0	16	Add 20 clocks per shift left Add 24 clocks per shift right Add 24 clocks for every shift performed Add 20 clocks per shift left; Add 24 clocks per shift right	
Shift Logical, Count in Register	SLR	R	6A	1	0/0	0/0	8		
Shift Arithmetic, Count in Register	SAR	R	6B	1	0/0	0/0	8		
Shift Cyclic, Count in Register	SCR	R	6C	1	0/0	0/0	8		
Double Shift Logical, Count in Register	DSLR	R	6D	1	0/0	0/0	12		
Double Shift Arithmetic, Count in Register	DSAR	R	6E	1	0/0	0/0	12		
Double Shift Cyclic, Count in Register	DSCR	R	6F	1	0/0	0/0	12		
INPUT/OUTPUT									
Execute I/O	XIO	IM,IMX IM,IMX	48 48	2 2	0/0 0/0	1/0 0/1	22 23	Input, Note 3 Output, Note 3	
Vectored I/O	VIO	D,DX D,DX D,DX	49 49 49	3 0 0	2/0 0/1 1/0	0/0 1/0 0/1	198 20 19		Add per input operation Add per output operation
Set Interrupt Mask	SMK		48	2	0/0	0/1	23		
Clear Interrupt Request	CLIR		48	2	0/0	0/1	23		
Enable Interrupts	ENBL		48	2	0/0	0/1	23		
Disable Interrupts	DSBL		48	2	0/0	0/1	23		
Reset Pending Interrupt	RPI		48	2	0/0	0/1	23		
Set Pending Interrupt Register	SPI		48	2	0/0	0/1	23		
Write Status Word	WSW		48	2	0/0	0/1	24		
Timer A Start	TAS		48	2	0/0	0/1	23		
Timer A Halt	TAH		48	2	0/0	0/1	23		
Output Timer A	OTA		48	2	0/0	0/1	29		
Timer B Start	TBS		48	2	0/0	0/1	23		
Timer B Halt	TBH		48	2	0/0	0/1	23		
Output Timer B	OTB		48	2	0/0	0/1	29		
Read Interrupt Mask	RMK		48	2	0/0	1/0	22		
Read Pending Interrupt Register	RPIR		48	2	0/0	1/0	22		
Read Status Word	RSW		48	2	0/0	1/0	22		
Read and Clear Fault Register	RCFR		48	2	0/0	1/0	22		
Input Timer A	ITA		48	2	0/0	1/0	23		
Input Timer B	ITB		48	2	0/0	1/0	23		
CONVERT									
Convert Floating Point to 16-Bit Integer	FIX	R	E8	1 1 1	0/0 0/0 0/0	0/0 0/0 0/0	35 27 23	Add 5 clocks per denormalization shift EO = 0 EO < 0	
Convert 16-Bit Integer to Floating Point	FLT	R	E9	1 1	0/0 0/0	0/0 0/0	47 24		Add 5 clocks per normalization shift MA = 0
Convert Extended Precision Floating Point to 32-Bit Integer	EFIX	R	EA	1 1 1	0/0 0/0 0/0	0/0 0/0 0/0	58 33 25		
Convert 32-bit Integer to Extended Precision Floating Point	EFLT	R	EB	1 1	0/0 0/0	0/0 0/0	48 26	Add 5 clocks per normalization shift MA = 0	

F - Number of instruction fetches
 R/W - Number of operand reads/writes
 I/O - Number of input/output operations
 C - Number of clock cycles
 MO - Floating point derived operand mantissa
 EO - Floating point 8-bit two's complement derived operand exponent
 MA - Floating point register accumulator mantissa
 EA - Floating point 8-bit two's complement register accumulator exponent
 DO - Derived operand

Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments
FLOATING POINT								
Extended-Precision Floating Point Load	EFL	D,DX	8A	2	3/0	0/0	20	
Extended-Precision Floating Point Store	EFST	D,DX	9A	2	0/3	0/0	23	
Floating Point Absolute Value of Register	FABS	R	AC	1	0/0	0/0	26	MO positive
				1	0/0	0/0	42	MO = 8000000
				1	0/0	0/0	32	MO > 8000000
Floating Point Negate Register	FNEG	R	BC	1	0/0	0/0	41	MO = 8000000 or MO = 400000
				1	0/0	0/0	36	
				1	0/0	0/0	18	MO = 0
Floating Point Compare	FCR	R	F9	1	0/0	0/0	24	EA > EO
				1	0/0	0/0	29	EA = EO
				1	0/0	0/0	19	EA < EO
	FCB	B	3C	1	2/0	0/0	32	EA > EO
				1	2/0	0/0	37	EA = EO
				1	2/0	0/0	27	EA < EO
	FCBX	BX	40D	1	2/0	0/0	32	EA > EO
				1	2/0	0/0	37	EA = EO
				1	2/0	0/0	27	EA < EO
	FC	D,DX	F8	2	2/0	0/0	36	EA > EO
				2	2/0	0/0	41	EA = EO
				2	2/0	0/0	31	EA < EO
Extended-Precision Floating Point Compare	EFCR	R	FB	1	0/0	0/0	24	EA > EO
				1	0/0	0/0	37	EA = EO
				1	0/0	0/0	19	EA < EO
	EFC	D,DX	FA	2	3/0	0/0	39	EA > EO
				2	3/0	0/0	48	EA = EO
				2	3/0	0/0	34	EA < EO
Floating Point Add	FAR	R	A9	1	0/0	0/0	84	MA < > 0, MO < > 0, Note 1
				1	0/0	0/0	58	MA = 0, MO < > 0, Note 1
				1	0/0	0/0	26	MA = 0, MO = 0, Note 1
	FAB	B	20	1	2/0	0/0	89	MA < > 0, MO < > 0, Note 1
				1	2/0	0/0	63	MA = 0, MO < > 0, Note 1
				1	2/0	0/0	31	MA = 0, MO = 0, Note 1
	FABX	BX	408	1	2/0	0/0	93	MA < > 0, MO < > 0, Note 1
				1	2/0	0/0	67	MA = 0, MO < > 0, Note 1
				1	2/0	0/0	31	MA = 0, MO = 0, Note 1
	FA	D,DX	A8	2	2/0	0/0	93	MA < > 0, MO < > 0, Note 1
				2	2/0	0/0	67	MA = 0, MO < > 0, Note 1
				2	2/0	0/0	35	MA = 0, MO = 0, Note 1
Extended-Precision Floating Point Add	EFAR	R	AB	1	0/0	0/0	103	MA < > 0, MO < > 0, Note 1
				1	0/0	0/0	76	MA = 0, MO < > 0, Note 1
				1	0/0	0/0	31	MA = 0, MO = 0, Note 1
	EFA	D,DX	AA	2	3/0	0/0	115	MA < > 0, MO < > 0, Note 1
				2	3/0	0/0	88	MA = 0, MO < > 0, Note 1
				2	3/0	0/0	43	MA = 0, MO = 0, Note 1
Floating Point Subtract	FSR	R	B9	1	0/0	0/0	83	MA < > 0, MO < > 0, Note 1
				1	0/0	0/0	57	MA = 0, MO < > 0, Note 1
				1	0/0	0/0	26	MA = 0, MO = 0, Note 1
	FSB	B	24	1	2/0	0/0	88	MA < > 0, MO < > 0, Note 1
				1	2/0	0/0	62	MA = 0, MO < > 0, Note 1
				1	2/0	0/0	31	MA = 0, MO = 0, Note 1
	FSBX	BX	409	1	2/0	0/0	92	MA < > 0, MO < > 0, Note 1
				1	2/0	0/0	66	MA = 0, MO < > 0, Note 1
				1	2/0	0/0	31	MA = 0, MO = 0, Note 1
	FS	D,DX	B8	2	2/0	0/0	92	MA < > 0, MO < > 0, Note 1
				2	2/0	0/0	66	MA = 0, MO < > 0, Note 1
				2	2/0	0/0	35	MA = 0, MO = 0, Note 1

F - Number of instruction fetches

R/W - Number of operand reads/writes

I/O - Number of input/output operations

C - Number of clock cycles

MO - Floating point derived operand mantissa

EO - Floating point 8-bit two's complement derived operand exponent

MA - Floating point register accumulator mantissa

EA - Floating point 8-bit two's complement register accumulator exponent

DO - Derived operand

Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments
FLOATING POINT								
Extended-Precision Floating Point Subtract	EFSR	R	BB	1	0/0	0/0	103	MA < > 0, MO < > 0, Note 1
				1	0/0	0/0	71	MA = 0, MO < > 0, Note 1
				1	0/0	0/0	31	MA = 0, MO = 0, Note 1
				2	3/0	0/0	115	MA < > 0, MO < > 0, Note 1
Floating Point Multiply	EFS	D,DX	BA	2	3/0	0/0	83	MA = 0, MO < > 0, Note 1
				2	3/0	0/0	43	MA = 0, MO = 0, Note 1
				1	0/0	0/0	165	Note 2
				1	0/0	0/0	38	MA = 0 or MO = 0, Note 2
	FMR	R	C9	1	0/0	0/0	173	Note 2
	FMB	B	28	1	2/0	0/0	46	MA = 0 or MO = 0, Note 2
	FMBX	BX	40A	1	2/0	0/0	173	Note 2
	FM	D,DX	C8	1	2/0	0/0	46	MA = 0 or MO = 0, Note 2
	EFMR	R	CB	2	2/0	0/0	177	Note 2
				2	2/0	0/0	50	MA = 0 or MO = 0, Note 2
Extended-Precision Floating Point Multiply	EFM	D,DX	CA	1	0/0	0/0	561	Note 2
				1	0/0	0/0	42	Note 2
				2	3/0	0/0	569	Note 2
				2	3/0	0/0	50	Note 2
Floating Point Divide	FDR	R	D9	1	0/0	0/0	251	
				1	0/0	0/0	34	Divisor = 0
				1	0/0	0/0	31	Dividend = 0
				1	0/0	0/0	43	Early overflow detect
	FDB	B	2C	1	2/0	0/0	255	
				1	2/0	0/0	38	Divisor = 0
				1	2/0	0/0	35	Dividend = 0
				1	2/0	0/0	47	Early overflow detect
	FDBX	BX	40B	1	2/0	0/0	255	
				1	2/0	0/0	38	Divisor = 0
				1	2/0	0/0	35	Dividend = 0
				1	2/0	0/0	47	Early overflow detect
	FD	D,DX	D8	2	2/0	0/0	259	
				2	2/0	0/0	42	Divisor = 0
				2	2/0	0/0	39	Dividend = 0
				2	2/0	0/0	51	Early overflow detect
Extended-Precision Floating Point Divide	EFDR	R	DB	1	0/0	0/0	743	
				1	0/0	0/0	43	Divisor = 0
	EFD	D,DX	DA	1	0/0	0/0	48	Dividend = 0
				2	3/0	0/0	759	
				2	3/0	0/0	59	Divisor = 0
				2	3/0	0/0	64	Dividend = 0

F - Number of instruction fetches
R/W - Number of operand reads/writes
I/O - Number of input/output operations
C - Number of clock cycles
MO - Floating point derived operand mantissa
EO - Floating point 8-bit two's complement derived operand exponent
MA - Floating point register accumulator mantissa
EA - Floating point 8-bit two's complement register accumulator exponent
DO - Derived operand

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Instruction Summary (Continued)

Operation	Mnemonic	Format	Op Code	F	R/W	I/O	C	Comments
LOGICAL								
Inclusive Logical OR	ORR	R	E1	1	0/0	0/0	4	
	ORB	B	30	1	1/0	0/0	13	
	ORBX	BX	40F	1	1/0	0/0	13	
	OR	D,DX	E0	2	1/0	0/0	12	
	ORIM	IM	4A08	2	0/0	0/0	8	
Logical AND	ANDR	R	E3	1	0/0	0/0	4	
	ANDB	B	34	1	1/0	0/0	13	
	ANDX	BX	40E	1	1/0	0/0	13	
	AND	D,DX	E2	2	1/0	0/0	12	
	ANDM	IM	4A07	2	0/0	0/0	8	
Exclusive Logical OR	XORR	R	E5	1	0/0	0/0	4	
	XOR	D,DX	E4	2	1/0	0/0	12	
	XORM	IM	4A09	2	0/0	0/0	8	
Logical NAND	NR	R	E7	1	0/0	0/0	8	
	N	D,DX	E6	2	1/0	0/0	16	
	NIM	IM	4A0B	2	0/0	0/0	12	
Set Bit	SBR	R	51	1	0/0	0/0	4	
	SB	D,DX	50	2	1/1	0/0	17	
	SBI	I,IX	52	2	2/1	0/0	22	
Reset Bit	RBR	R	54	1	0/0	0/0	4	
	RB	D,DX	53	2	1/1	0/0	17	
	RBI	I,IX	55	2	2/1	0/0	22	
Test Bit	TBR	R	57	1	0/0	0/0	4	
	TB	D,DX	56	2	1/0	0/0	12	
	TBI	I,IX	58	2	2/0	0/0	17	
Test and Set Bit	TSB	D,DX	59	2	1/1	0/0	17	
Set Variable Bit in Register	SVBR	R	5A	1	0/0	0/0	8	
Reset Variable Bit in Register	RVBR	R	5C	1	0/0	0/0	8	
Test Variable Bit in Register	TVBR	R	5E	1	0/0	0/0	8	
Store Register through Mask	SRM	D,DX	97	2	1/1	0/0	25	
STACK								
Stack IC and Jump to Subroutine	SJS	D,DX	7E	2	0/1	0/0	17	
Unstack IC and Return from Subroutine	URS	S	7F	2	1/0	0/0	17	
Pop Multiple Registers Off the Stack	POPM	S	8F	1	2/0	0/0	17	Add 4 clocks for each register pop
Push Multiple Registers onto the Stack	PSHM	S	9F	1	0/1	0/0	12	Add 5 clocks for each push
SPECIAL								
Move Multiple Words, Memory-to-Memory	MOV	S	93	1	0/0	0/0	8	Add 22 clocks for every word moved
Exchange Words in Registers	XWR	R	ED	1	0/0	0/0	12	
Load Status	LST	D	7D	2	3/0	0/0	35	
		DX	7D	2	3/0	0/0	39	
	LSTI	I	7C	2	4/0	0/0	40	
		IX	7C	2	4/0	0/0	43	
No Operation	NOP	S	FF	1	0/0	0/0	4	
Break Point	BPT	S	FFFF	1	0/0	0/0	8	
Built-in Function	BIF	S	4F	1	0/0	0/0	16	

F – Number of instruction fetches

R/W – Number of operand reads/writes

I/O – Number of input/output operations

C – Number of clock cycles

MO – Floating point derived operand mantissa

EO – Floating point 8-bit two's complement derived operand exponent

MA – Floating point register accumulator mantissa

EA – Floating point 8-bit two's complement register accumulator exponent

DO – Derived operand

Notes:

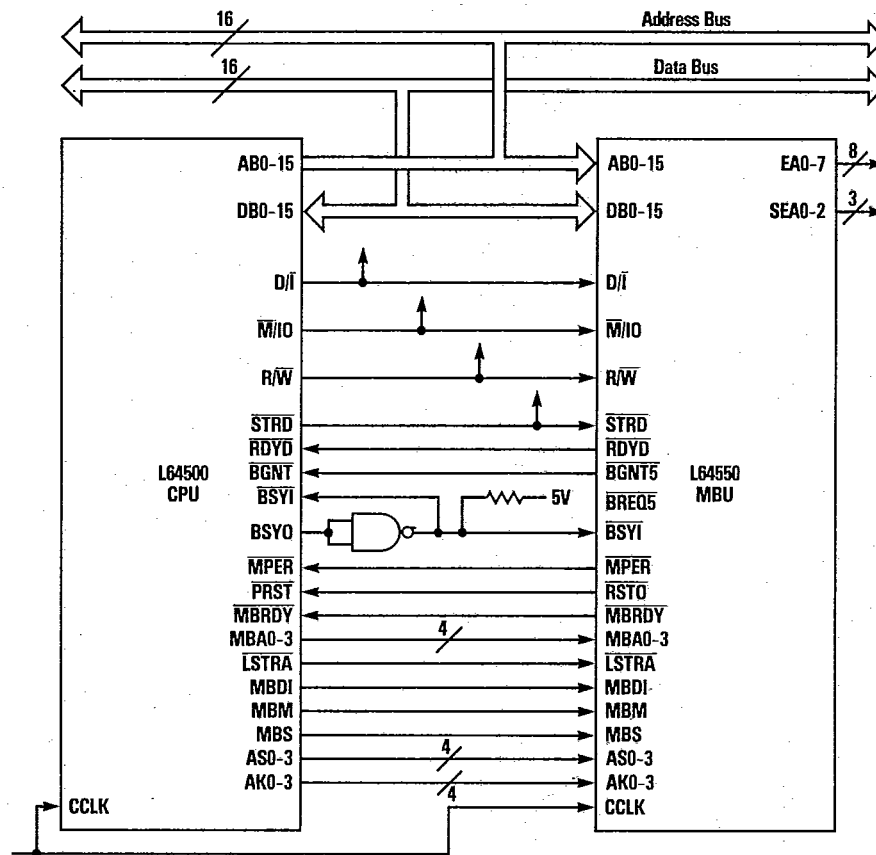
1. Add 5 clocks for every operand alignment postnormalization shift required.
2. Add 5 clocks for every postnormalization shift required.
3. All external I/O operations including L64550 MBU related commands.

Applications Information

The following general information exists for:

- L64500 CPU and L64550 MBU connection diagram
- Bus Arbitration general information
- L64500 CPU connection to a DMA device with functional timing diagram
- L64550 MBU Bus Arbitration Connection for Multiple L64500 CPUs and DMA Devices
- DMA, Bus Master Controller and Arbitration for L64500 CPU/DMA Configuration

L64500 CPU and L64550 MBU Connection Diagram

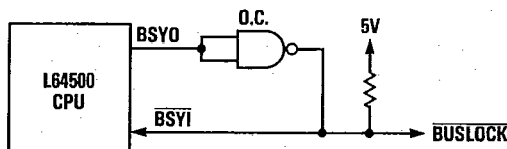


Bus Arbitration

A simple bus arbitration scheme uses three bus control signals:

- **BUSREQ** – This signal is generated by any Bus Master requiring the bus. The L64500 CPU **BUSREQ** signal is **BREQ**.

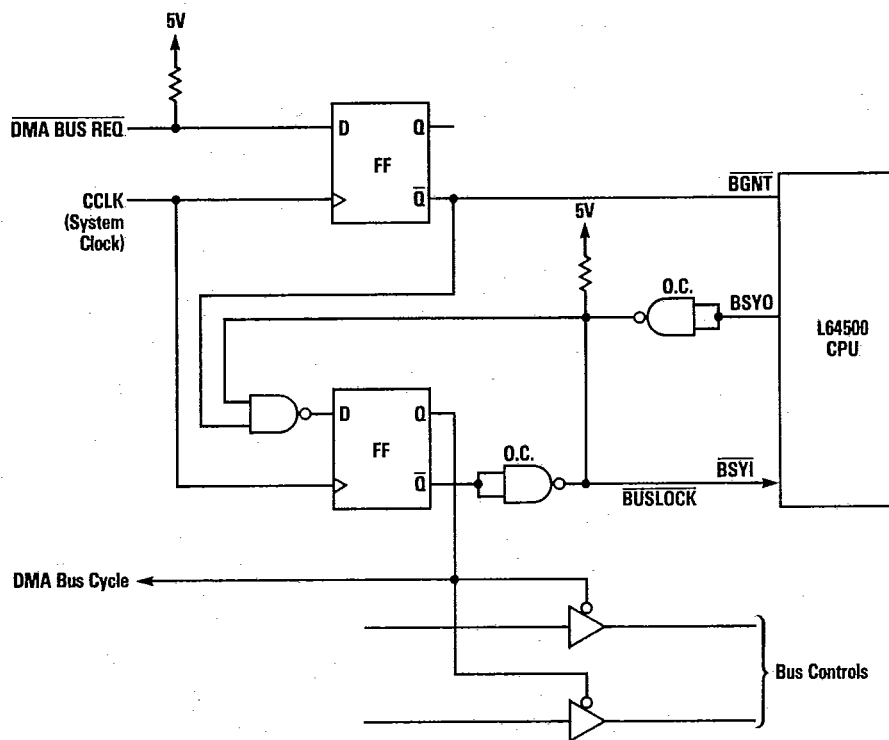
- **BUSGNT** – This signal is generated by the arbiter to the requester with the highest priority. The L64500 CPU **BUSGNT** signal is **BGNT**.
- **BUSLOCK** – This signal is generated by any bus master indicating that the bus is unavailable to other bus contenders. The L64500 CPU **BUSLOCK** signal is **BSYO** and **BSYI** connected as shown below.



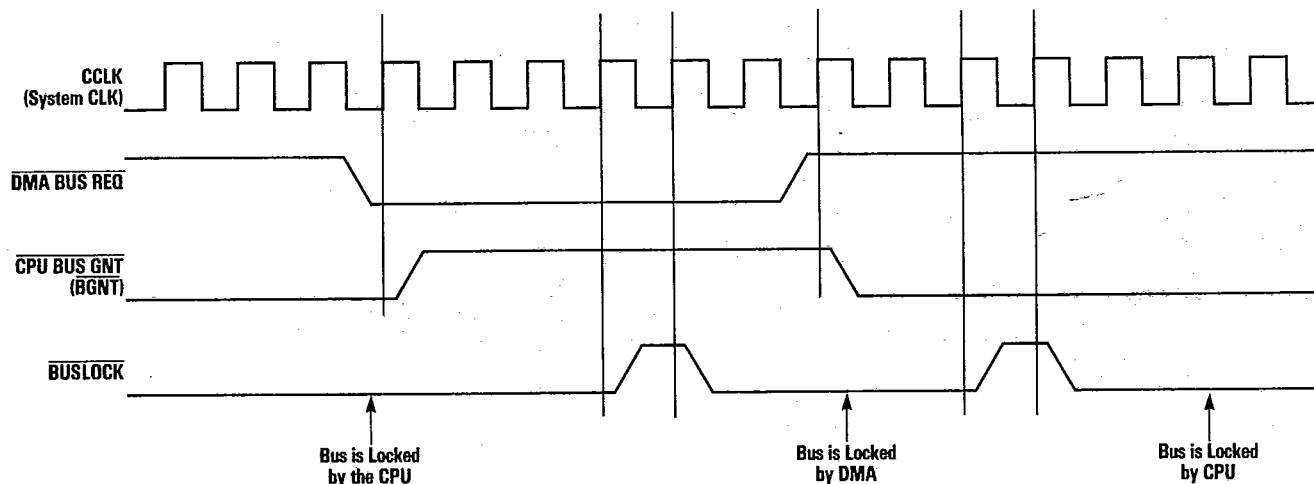
Applications Information (Continued)

L64500 CPU/DMA Connection

- The DMA device generates the **BUSREQ** signal.
- The bus arbiter will respond with the signal **BUSGNT**.
- Upon receiving **BUSGNT**, the DMA device must wait until **BUSLOCK** becomes inactive.

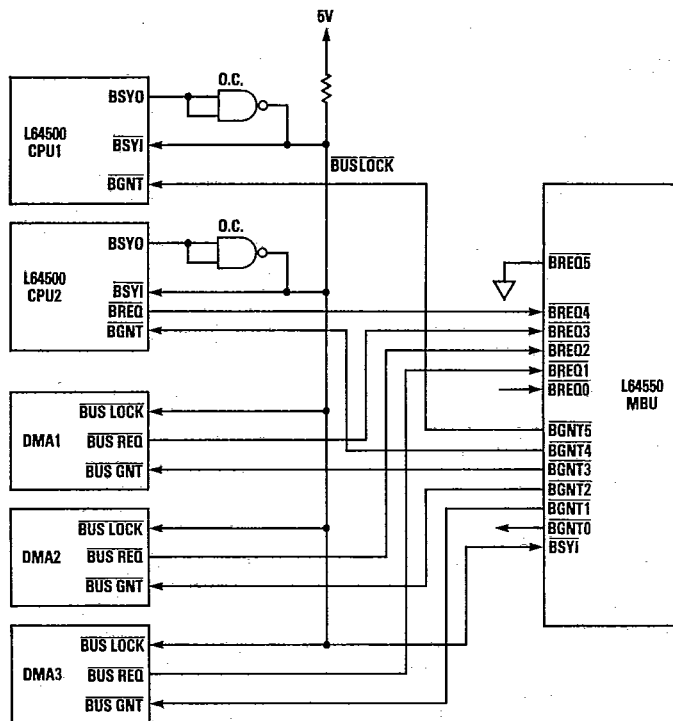


L64500 CPU/DMA Bus Arbitration

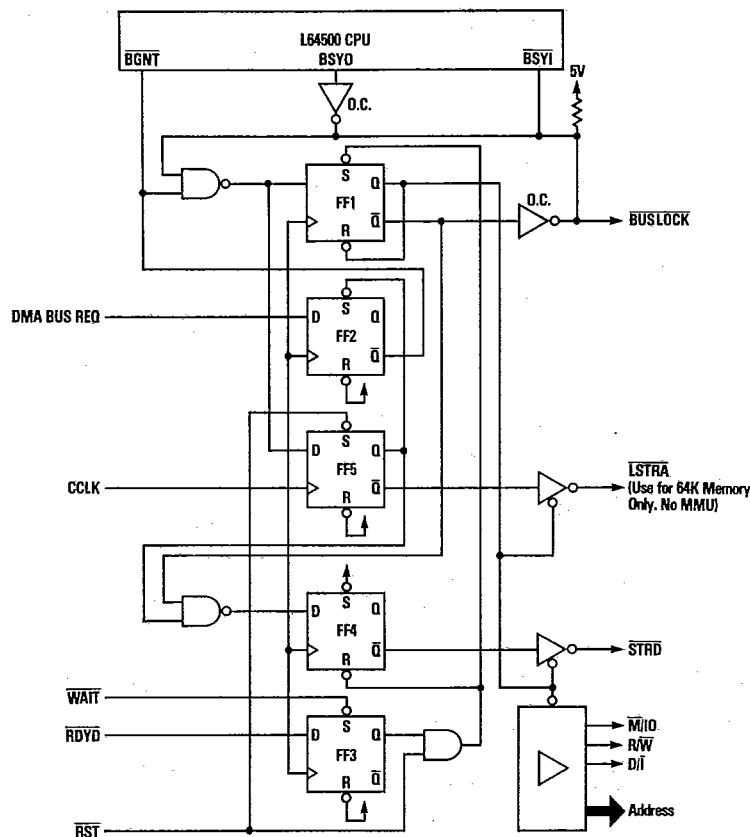


CPU/DMA Bus Arbitration Functional Timing

Applications Information
(Continued)



L64550 MBU Bus Arbitration Connection for Multiple L64500 CPUs and DMA Devices



DMA, Bus Master Controller and Arbitration for CPU/DMA Configuration

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Operating Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	±10	mA
Storage Temperature Range (Ceramic)	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Military	TA	-55 to +125	°C

DC Characteristics: VDD = 5 V ± 10%, TA = -55°C to +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL	Voltage Input LOW				0.8	V
VIH	Voltage Input HIGH		2.25			V
IIL	Input Current LOW		-100	-30	-8	μA
IIH	Input Current HIGH				40	μA
VOH	Voltage Output HIGH DB0-15, AK0-3, AS0-3, CP, HLDK, TST01,2, MBS, PWRUP, SNI, MERR IXRD, INTSTF, MBDI, MBM All Others	IOH = -3.2 mA IOH = -6.4 mA	2.4	4.5		V
VOL	Voltage Output LOW DB0-15, AK0-3, AS0-3, CP, HLDK, TST01,2, MBS, PWRUP, SNI, MERR IXRD, INTSTF, MBDI, MBM All Others	IOL = 3.2 mA IOL = 6.4 mA		0.2	0.4	V
IOZ	3-State Output Leakage Current	VOH = VSS or VDD	-10	±1	10	μA
IOS	Output Short Circuit Current ⁽¹⁾	VDD = Max, VO = VDD VDD = Max, VO = 0 V	15 -5	50 -25	130 -100	mA mA
IDD	Supply Current	CLK = 25 MHz, CL = 50 pF			100	mA

Note: Not more than one output may be shorted at a time for a maximum duration of one second.

IMPORTANT:

All 3-state outputs should contain pullup resistors. Recommend for 3.2 mA outputs: 2.2 KΩ, for 6.4 mA outputs: 1.0 KΩ-1.5 KΩ.

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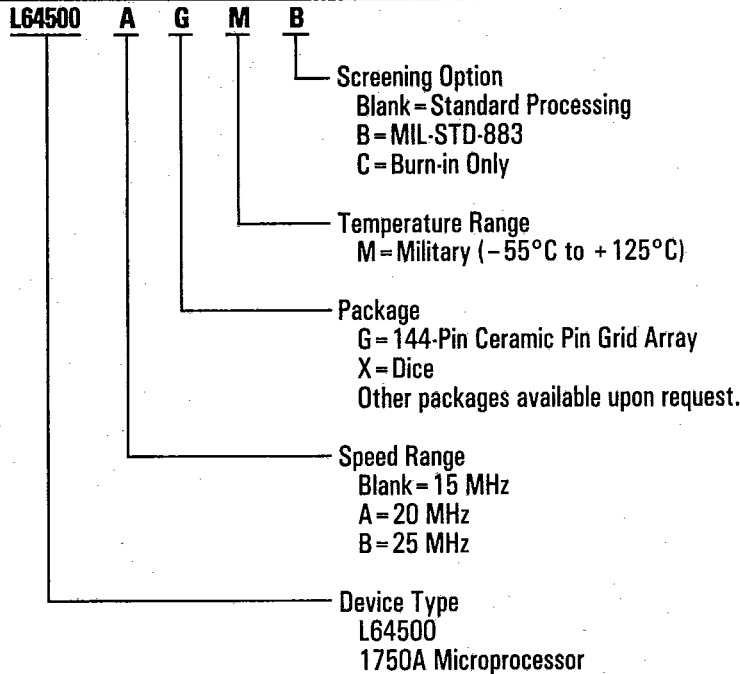
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Ordering Information



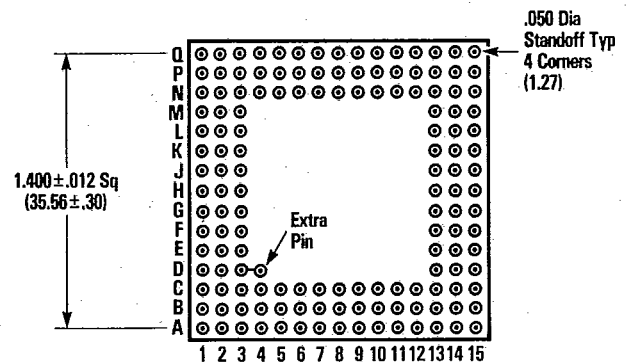
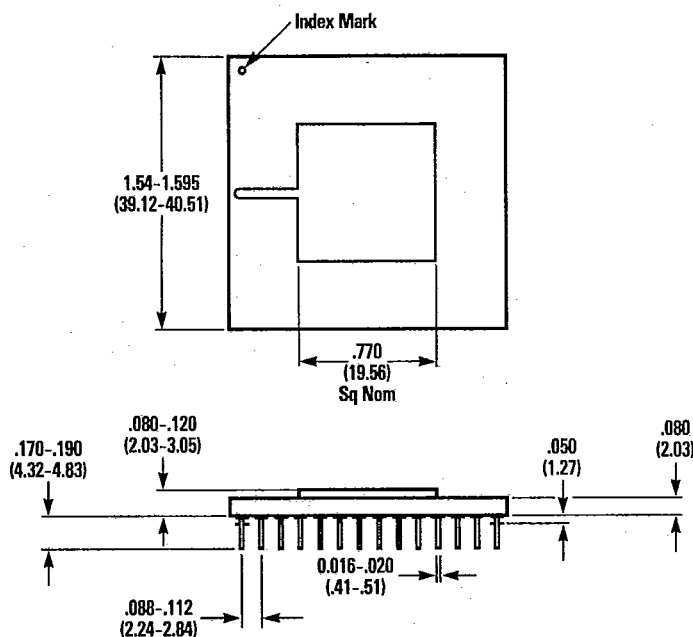
Valid Options

GMB, GM
 XMB, XM

Packaging

Initially, the L64500 will be offered in a 144-Pin Grid Array (PGA). The mechanical drawings and dimensions of the package are shown in Figure 10. This package was selected because of its easier breadboarding characteristics. If other package types are required, easy conversion is possible. The different package

types available to use are governed by the die cavity and available pins. LSI Logic provides package selector guides for alternative packaging such as Leaded or Leadless chip carriers. Customer unique package requirements can be handled, but must be reviewed by the LSI Logic packaging group.



Notes: Brim standoff at 4 corners standard. Extra pin connected to pin D3.

Figure 10. 144-Pin Ceramic Pin-grid Array

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Screening Options

The L64500 can be selected as evaluation or production units. Evaluation units have been screened to commercial standards but have the full -55°C to 125°C military temperature specification. These units are not recommended for use in military production environments.

Production units can be ordered to commercial standards, MIL-STD-883C, Class B and Class S. Contact factory for screening details.

LSI Logic Design System (LDS)

The L64500 can be used with LSI Logic's Design System (LDS) simulation tools as a library element. This unique feature allows the user to develop a full MIL-STD-1750A system environment in software. This environment allows the user to develop accurate systems and sophisticated MIL-STD-1750A associated Application Specific Integrated Circuits (ASIC) offered by LSI Logic. In addition, the user can increase the

functionality of the L64500 by adding other circuitry to the L64500 library element making the design an enhanced one chip solution. To use this feature, the LSI Logic LDS environment can be licensed or can be accessed through one of LSI Logic's design centers identified on the last page. Training on the LDS system lasts three days.

Szwerenko Benchmark Approach

The characteristics of the applications in today's military computer systems are so diverse that a single instruction mix provides little useful information when selecting a processor. The Szwerenko benchmark program was built from a number of representative modules and performs a least squares fit of the modules to a set of target statistics based on the accepted DAIS mix. Since the DAIS mix does not include frequently-used constructs, such as the SOJ loop counter, and subroutine overhead instructions like linkage and register pushes and pops, the mix was modified to include these instructions.

The Szwerenko/SEAFAC benchmark program measures and reports the performance of the unit under test on eight diverse modules and also provides a single aggregate performance figure. Furthermore, the program measures and reports a 'typical' interrupt overhead figure.

Table 3 provides the target and the expected statistics as a result of the solution of the system of equations. It is important to note that the actual runtime statistics will vary because the benchmark generates a timer interrupt every 1 ms to simulate an actual runtime environment.

Table 3. Statistics for Szwerenko/SEAFAC Benchmark

	Target	Solution	Error
Load/Store	38.73%	38.75%	0.06%
Branch*	21.00%	20.83%	0.82%
Compare	8.56%	8.51%	0.57%
Add/Subtract Fixed	6.05%	5.96%	0.73%
Multiply Floating	5.15%	5.12%	0.55%
PSHM/POPM/MOV	5.00%	5.07%	1.49%
Add/Subtract Floating	4.08%	3.99%	2.27%
Call	4.00%	3.76%	6.03%
Multiply Fixed	1.63%	1.83%	12.53%
Shift	1.63%	1.68%	3.17%
Logical	1.63%	1.69%	3.38%
Bit	1.63%	1.67%	2.35%
Divide Floating	0.57%	0.77%	34.79%
Divide Fixed	0.33%	0.37%	13.10%

*Includes SOJ

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Szewerenko Benchmark Approach (Continued)

In actual use, a user will focus on those modules which they believe most closely match the target application. Listed below are the eight modules describing their emphasis.

- The Whetstone module is a good indication of general numerical capability.
- The Coordinate Conversion module is a good indicator of floating point performance.
- The Interrupt Overhead test gives an idea of how fast context changes can be made.

- The Kalman Filter performs integer arithmetic and a number of subroutine calls.
- The ASCII to Dot Matrix, Bit Matrix Transpose and Cyclic Redundancy Check modules perform register intensive non-arithmetic operations.
- The Heapsort module does data movement and comparisons on a moderate sized address space.

The benchmark results for the L64500 CPU and L64550 MBU system are reported in Table 4.

Table 4. The L64500 CPU and L64550 MBU Performance Test Summary for Various System Operating Frequencies

Test Modules	15 MHz	20 MHz	25 MHz	30 MHz	Units
Bit Matrix Transpose	1541	2315	2881	3457	KOPS
Cyclic Redundancy Check Calculation	1088	1569	1974	2368	KOPS
ASCII String to Dot Matrix Conversion	790	1141	1427	1712	KOPS
JTIDS Accept/Hash/Store	760	1123	1400	1680	KOPS
Heapsort	1097	1619	2022	2426	KOPS
Fixed-point Kalman Filter	542	774	966	1159	KOPS
Standard Precision Whetstone	340	465	579	694	KOPS
Lat/Long to Flat Coordinate Conversion	277	381	475	570	KOPS
Typical Interrupt Overhead	18	12	10	9	μsecs
The Szewerenko/SEAFAC Performance	490	689	859	1030	KOPS

Statistics for the individual modules are available. Contact our local sales office.