

512K-BIT[64Kx8] CMOS MULTIPLE-TIME-PROGRAMMABLE ROM

FEATURES

- 64K x 8 organization
- +5V operating power supply
- +12.5V program/erase voltage
- Electric erase instead of UV light erase
- Fast access time: 70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible

- Operating current: 30mA
- Standby current: 100 μ A
- 100 minimum erase/program cycles
- Package type:
 - 28 pin plastic DIP
 - 28 pin SOP
 - 32 pin PLCC
 - 28 pin TSOP(II)

PATENTED TECHNOLOGY

GENERAL DESCRIPTION

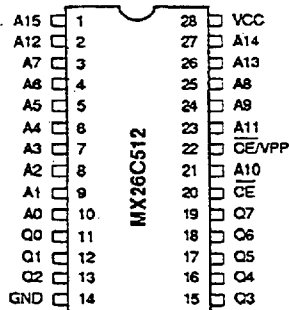
The MX26C512 is a 5V, 512K-bit, MTP ROM™ (Multiple Time Programmable Read Only Memory). It is organized as 64K words by 8 bits per word, operates from a +5 volt supply, has a static standby mode, and features fast single address location programming. It is designed to be reprogrammed and erased by an EPROM programmer or on-board. All programming/erasing signals are TTL

levels, requiring a single pulse. The MX26C512 supports an intelligent quick pulse programming algorithm which can result in a programming time of less than 30 seconds.

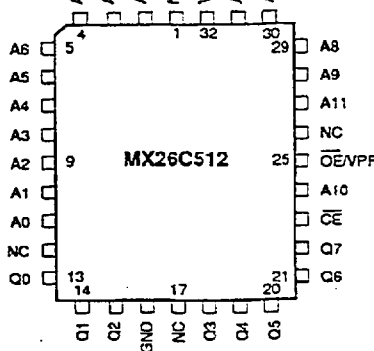
This MTP ROM™ is packaged in industry standard 28 pin dual-in-line packages, 32 pin PLCC packages or 28 pin TSOP packages and 28 pin SOP packages.

PIN CONFIGURATIONS

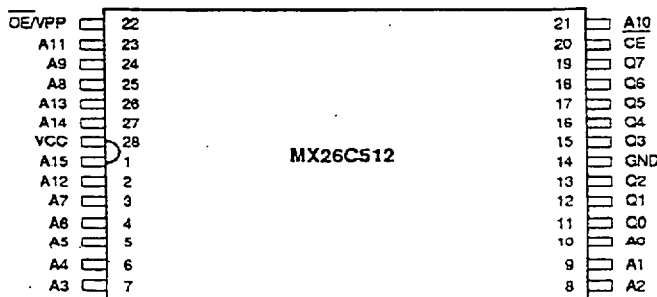
PDIP/SOP



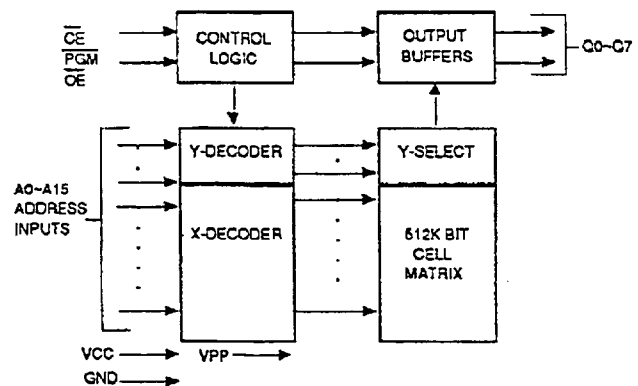
PLCC



TSOP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0-A15	Address Input
Q0-Q7	Data Input/Output
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

FUNCTIONAL DESCRIPTION

When the MX26C512 is delivered, or it is erased, the chip has all 512K bits in the "ONE", or HIGH state. "ZEROS" are loaded into the MX26C512 through the procedure of programming.

PROGRAMMING MODE

ON-BOARD PROGRAMMING ALGORITHM

The MX26C512 is programmed by an EPROM programmer or on-board. The device is set up in the programming mode when the programming voltage $\overline{OE}/VPP = 12.5V$ is applied, with $VCC = 5V$ (Algorithm shown in Figure 1). Programming is achieved by applying a single TTL low level 100 μs pulse to the $\overline{CE}$ input after addresses and data lines are stable. If the data is not verified, additional pulses are applied for a maximum of 20 pulses. After the data is verified, one 100 μs pulse is applied to overprogram the byte so that program margin is assured. This process is repeated while sequencing through each address of the device. When programming is completed, the data at all the addresses are verified at $VCC = 5V \pm 10\%$.

The VCC supply of the MXIC On-Board Programming Algorithm is designed to be $5V \pm 10\%$ particularly to facilitate the programming operation under the on-board application environment. But it can also be implemented in an industrial-standard EPROM programmer.

COMPATIBILITY WITH MX27C512 FAST PROGRAMMING ALGORITHM

Besides the On-Board Programming Algorithm, the Fast Programming Algorithm of MX27C512 also applies to MX26C512. MXIC Fast Algorithm is the conventional EPROM programming algorithm and is available in industrial-standard EPROM programmers. A user of industrial-standard EPROM programmer can choose either of the algorithms base on his preference.

The device is set up in the fast programming mode when the programming voltage $\overline{OE}/VPP = 12.75V$ is applied, with $VCC = 6.25V$, (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100 μs pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at $VCC = 5V \pm 10\%$.

ERASE MODE

The MX26C512 is erased by EPROM programmer or in-system. The device is set up in erase mode when $A9 = 12.5V$ and $\overline{OE}/VPP = 12.5V$ are applied, with $VCC = 5V$. (Algorithm is shown in Figure 3). The erase time is around 1sec. If the erase is not verified, an additional erase processes will be repeated for a maximum of 60 times.

PROGRAM INHIBIT MODE

Programming of multiple MX26C512 in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX26C512 may be common. A TTL low-level program pulse applied to an MX26C512 $\overline{CE}$ input with $\overline{OE}/VPP = 12.5 \pm 0.5 V$ will program that MX26C512. A high-level $\overline{CE}$ input inhibits the other MX26C512 from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}/VPP$ and $\overline{CE}$, at VIL. Data should be verified tDV after the falling edge of $\overline{CE}$.

ERASE VERIFY MODE

Verification should be performed on the erased chip to determine that whole chip(all bits) was correctly erased. Verification should be performed with $\overline{OE}/VPP$ and $\overline{CE}$ at VIL and $VCC = 5V$.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from a MTP that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}C \pm 5^{\circ}C$ ambient temperature range that is required when programming the MX26C512.

To activate this mode, the programming equipment must force $12.0 \pm 0.5 V$ on address line A9 of the device. Two identifier bytes may then be sequenced from the device

outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX26C512, these two identifier bytes are given in the Mode Select Table. All identifiers for the manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX26C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX26C512 has a CMOS standby mode which reduces the maximum VCC current to 100 μ A. It is placed in CMOS standby when $\overline{CE}$ is at VCC $\pm$ 0.3 V. The MX26C512 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and

connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μ F bulk electrolytic capacitor should be used between VCC and GND for each of the eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

MODE	PINS				OUTPUTS
	$\overline{CE}$	$\overline{OE/VPP}$	A0	A9	
Read	VIL	VIL	X	X	DOUT
Output Disable	VIL	VIH	X	X	High Z
Standby (TTL)	VIH	X	X	X	High Z
Standby (CMOS)	VCC	X	X	X	High Z
Program	VIL	VPP	X	X	DIN
Program Verify	VIL	VIL	X	X	DOUT
Erase	VIL	VPP	X	VH	HIGH Z
Erase Verify	VIL	VIL	X	X	DOUT
Program Inhibit	VIH	X	X	X	High Z
Manufacturer Code	VIL	VIL	VIL	VH	C2H
Device Code(26C512)	VIL	VIL	VIH	VH	DIH

NOTES: 1. VH = 12.0 V $\pm$ 0.5 V

2. X = Either VIH or VIL(For auto select)

3. A1 - A8 = A10 - A15 = VIL(For auto select)

4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. ON-BOARD PROGRAMMING FLOW CHART

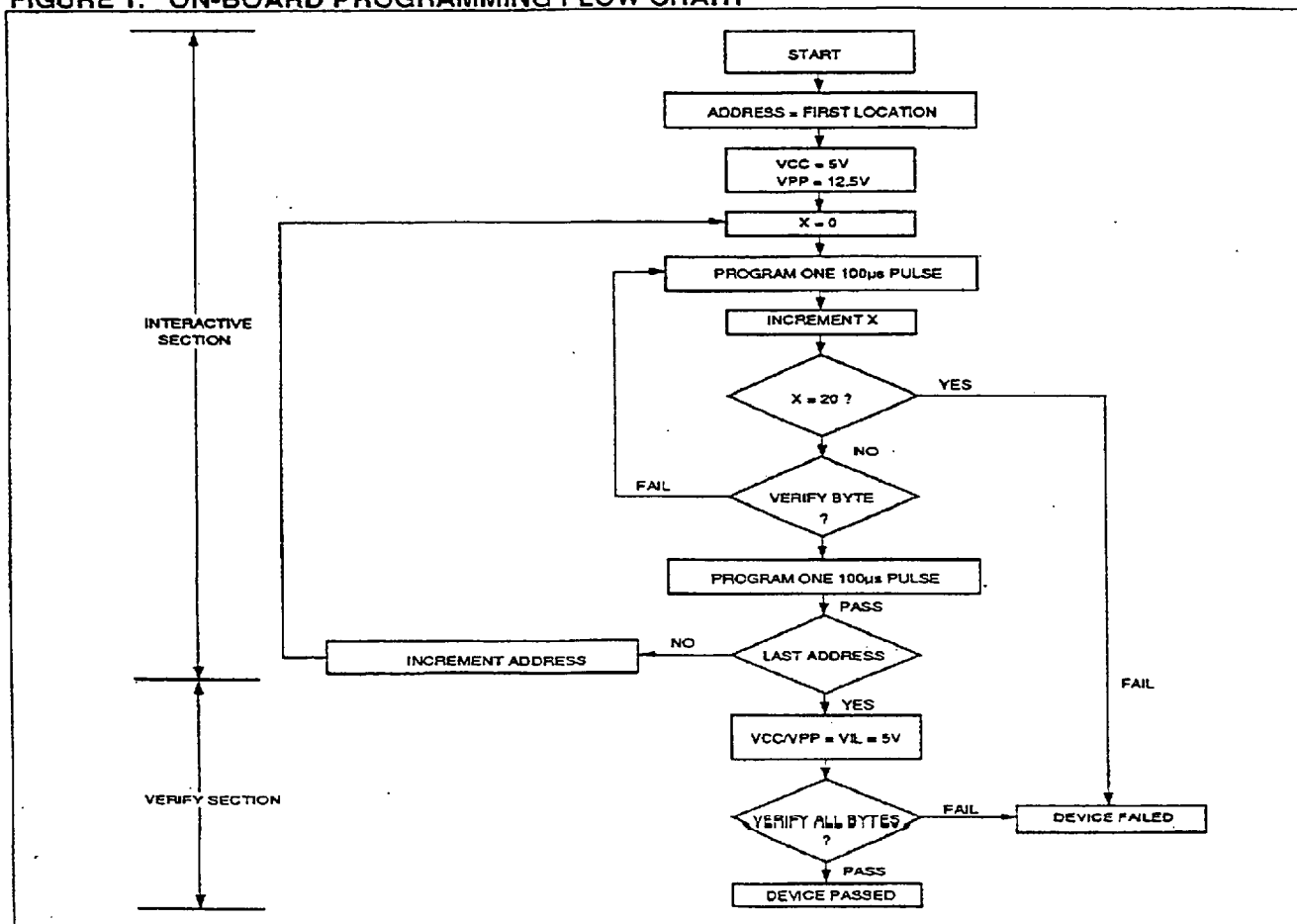


FIGURE 2. COMPATIBILITY WITH MX27C512 FAST PROGRAMMING FLOW CHART

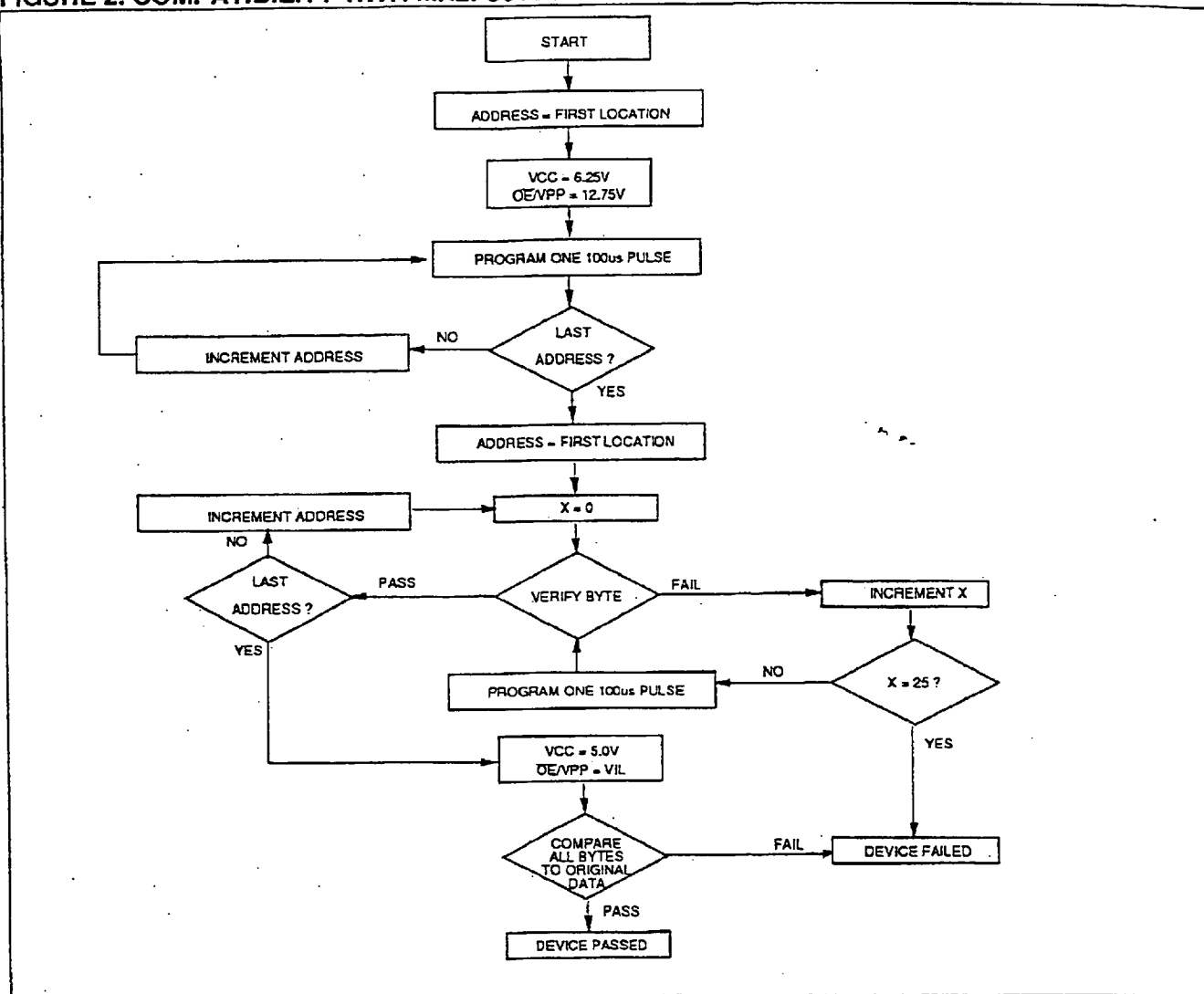
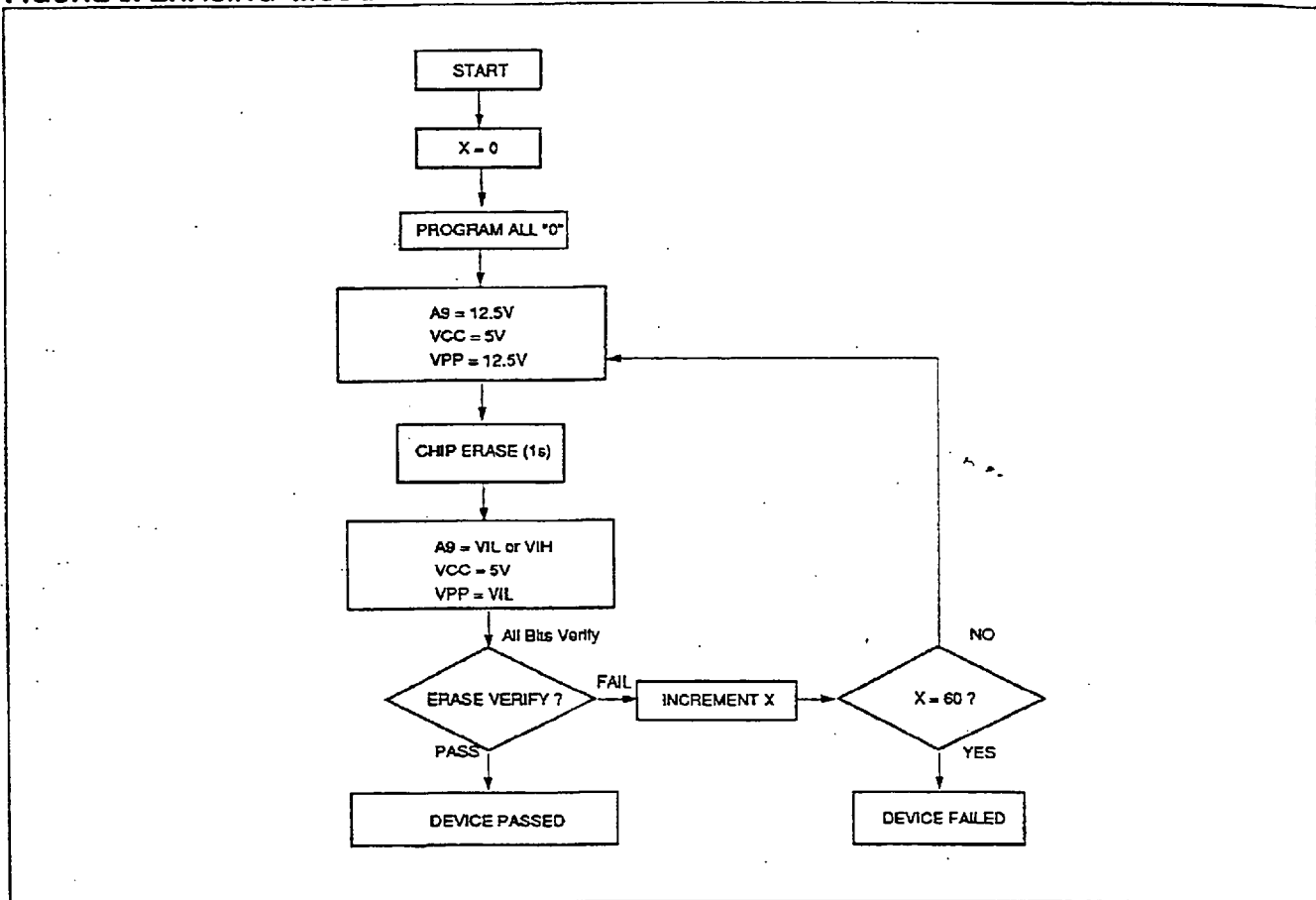
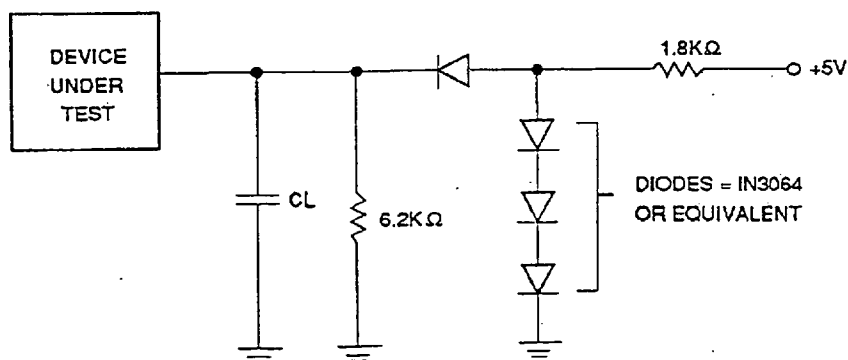


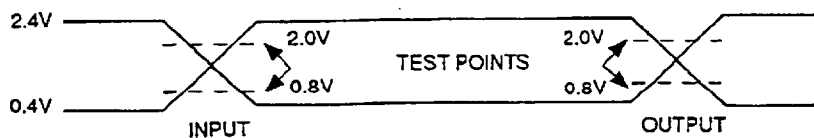
FIGURE 3. ERASING MODE FLOW CHART


SWITCHING TEST CIRCUITS

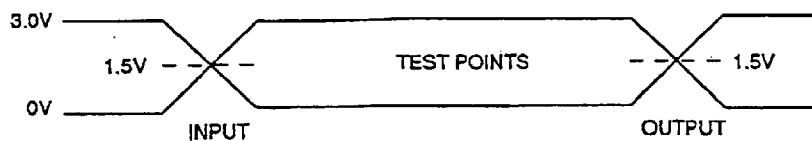


CL = 100 pF including jig capacitance(30pF for 70 ns parts)

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
Input pulse rise and fall times are ≤ 10 ns.



AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤ 10 ns.
(2) For MX26C512-70

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	μA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	μA	$\overline{CE} = VCC \pm 0.3V$
ICC2	VCC Standby Current		1.5	mA	$\overline{CE} = VIH$
ICC1	VCC Active Current		30	mA	CE = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	μA	$\overline{CE} = \overline{OE} = VIL, VPP = 5.5V$

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	8	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	26C512 -70		26C512 -90		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		70		90	ns	$\overline{CE} = \overline{OE} = \text{VIL}$
tCE	Chip Enable to Output Delay		70		90	ns	$\overline{OE} = \text{VIL}$
tOE	Output Enable to Output Delay		35		40	ns	$\overline{CE} = \text{VIL}$
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	20	0	25	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		ns	

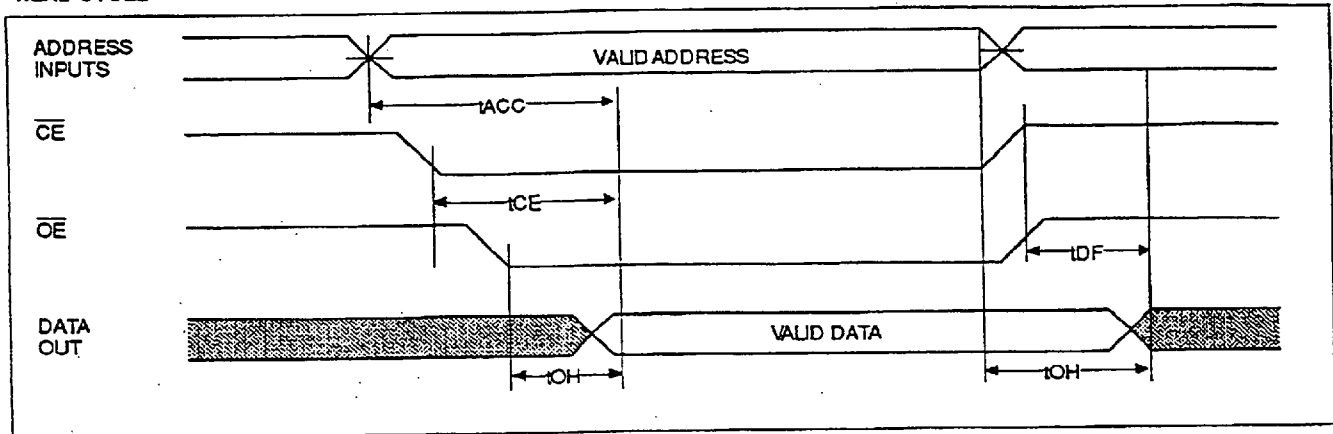
SYMBOL	PARAMETER	26C512 -10		26C512 -12		26C512 -15		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		100		120		150	ns	$\overline{CE} = \overline{OE} = \text{VIL}$
tCE	Chip Enable to Output Delay		100		120		150	ns	$\overline{OE} = \text{VIL}$
tOE	Output Enable to Output Delay		45		50		65	ns	$\overline{CE} = \text{VIL}$
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

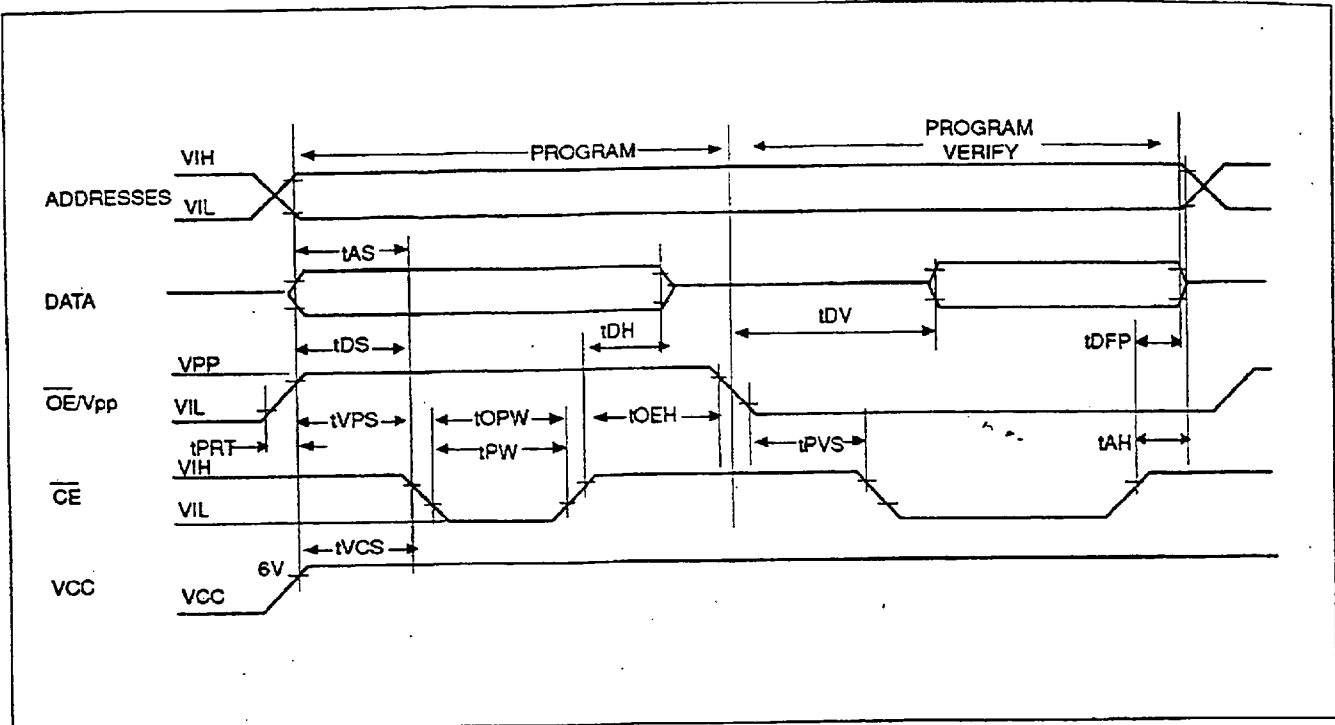
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program/Erase & Verify)		50	mA	
IPP2	VPP Supply Current(Program)/Erase		50	mA	$\overline{CE} = \text{PGM} = \text{VIL}$, $\overline{OE} = \text{VIH}$
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	
IPP A9	A9 Auto Select Current /Erase		1	mA	$\overline{CE} = \text{PGM} = \text{VIL}$, $\overline{OE} = \text{VIH}$

AC PROGRAMMING CHARACTERISTICS $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

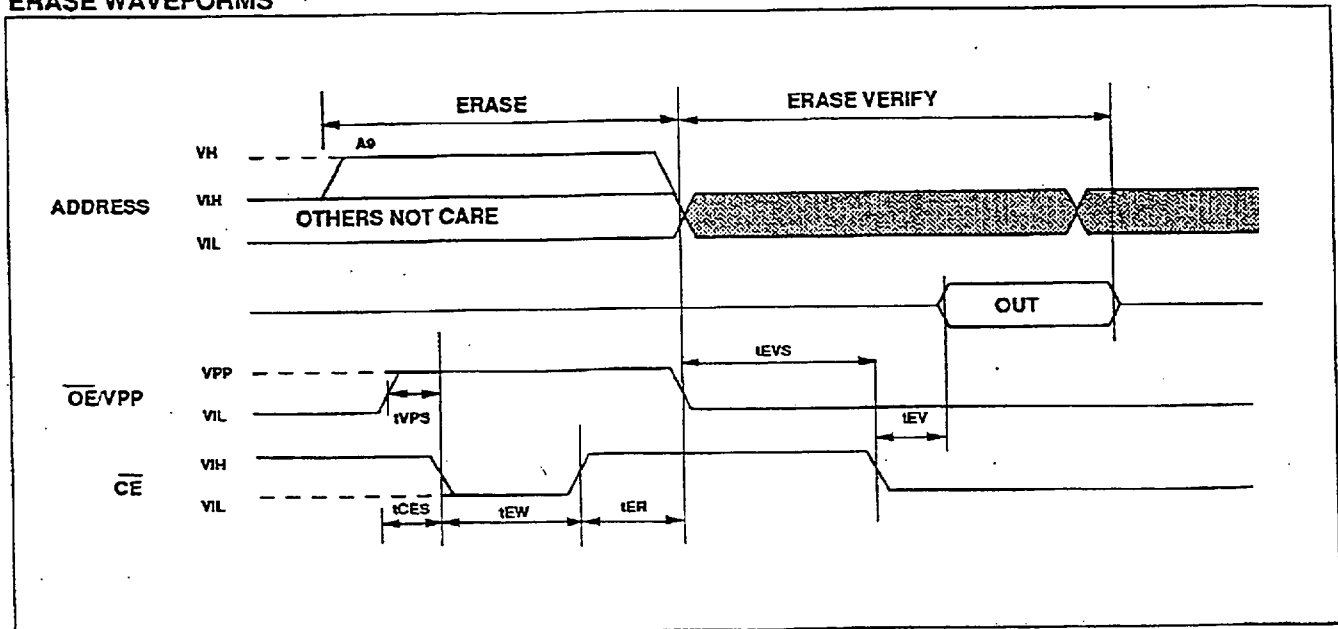
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
t_{AS}	Address Setup Time	2.0		μS	
t_{OES}	$\overline{\text{OE}}$ Setup Time	2.0		μS	
t_{DS}	Data Setup Time	2.0		μS	
t_{AH}	Address Hold Time	0		μS	
t_{DH}	Data Hold Time	2.0		μS	
t_{DFP}	$\overline{\text{CE}}$ to Output Float Delay	0	130	nS	
t_{VPS}	VPP Setup Time	2.0		μS	
t_{PW}	Program Pulse Width	95	105	μS	
t_{VCS}	VCC Setup Time	2.0		μS	
t_{DV}	Data Valid from $\overline{\text{CE}}$		250	nS	
t_{CES}	$\overline{\text{CE}}$ Setup Time	2.0		μS	
t_{OE}	Data valid from $\overline{\text{OE}}$		150	nS	
t_{ER}	Erase Recovery Time	0.5		S	
t_{EW}	Erase Pulse Width	1		S	
t_{EV}	Erase Verify Time		200	nS	
t_{A9S}	A9 Setup Time	2.0		μS	

WAVEFORMS
READ CYCLE


PROGRAMMING WAVEFORMS



ERASE WAVEFORMS



ORDERING INFORMATION
PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX26C512PC-70	70	30	100	28 Pin DIP
MX26C512MC-70	70	30	100	28 Pin SOP
MX26C512QC-70	70	30	100	32 Pin PLCC
MX26C512TC-70	70	30	100	28 Pin TSOP(I)
MX26C512PC-90	90	30	100	28 Pin DIP
MX26C512MC-90	90	30	100	28 Pin SOP
MX26C512QC-90	90	30	100	32 Pin PLCC
MX26C512TC-90	90	30	100	28 Pin TSOP(I)
MX26C512PC-10	100	30	100	28 Pin DIP
MX26C512MC-10	100	30	100	28 Pin SOP
MX26C512QC-10	100	30	100	32 Pin PLCC
MX26C512TC-10	100	30	100	28 Pin TSOP(I)
MX26C512PC-12	120	30	100	28 Pin DIP
MX26C512MC-12	120	30	100	28 Pin SOP
MX26C512QC-12	120	30	100	32 Pin PLCC
MX26C512TC-12	120	30	100	28 Pin TSOP(I)
MX26C512PC-15	150	30	100	28 Pin DIP
MX26C512MC-15	150	30	100	28 Pin SOP
MX26C512QC-15	150	30	100	32 Pin PLCC
MX26C512TC-15	150	30	100	28 Pin TSOP(I)

Revision History

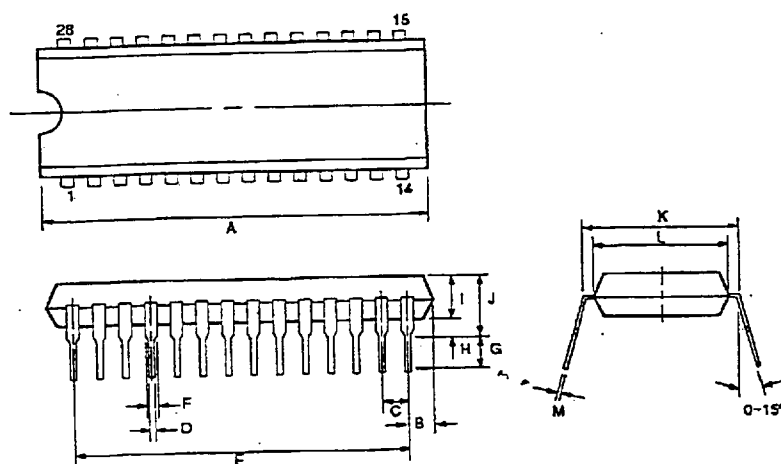
Revision#	Description
1.2	Add 28 pin TSOP and SOP packages.
1.3	Erasing mode flow chart: Chip erase (5s)----> (1s). Programming waveforms: $\overline{CE}$ changed.

PACKAGE INFORMATION

28-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	37.34 max	1.470 max
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	32.99	1.300
F	1.52 [Typ.]	.060 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.84 ± .25	.545 ± .010
M	.25 [Typ.]	.010 [Typ.]

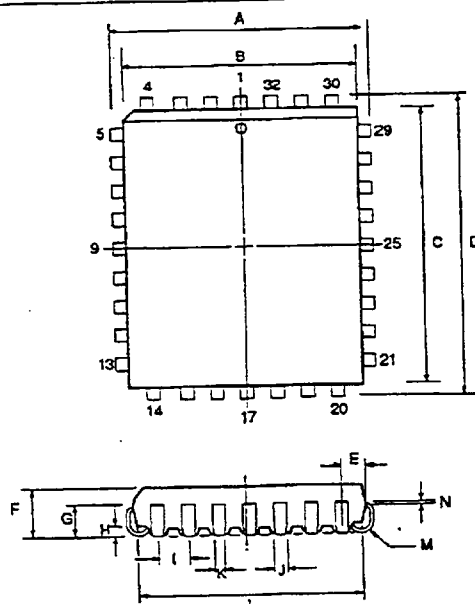
NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position [TP] at maximum material condition.



32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89 R	.035 R
N	.25 (TYP.)	.010 (TYP.)

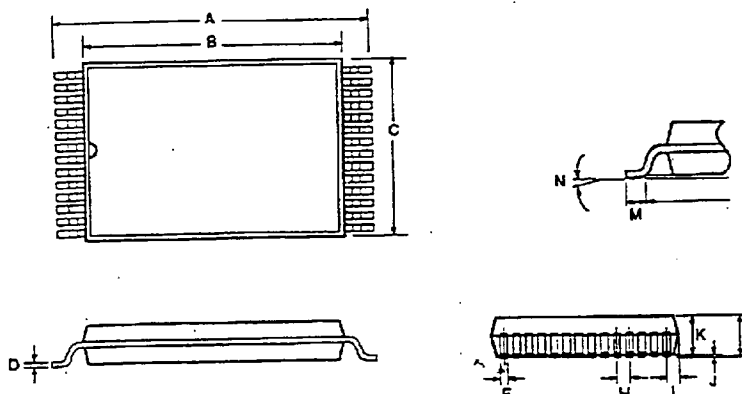
NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position [TP] at maximum material condition.



28-PIN PLASTIC TSOP

ITEM	MILLIMETERS
A	13.4 ± .2
B	11.8 ± .1
C	8.0 ± .1
D	.15 ± .01
F	2 ± .03
H	.55 [Typ.]
I	.425 [Typ.]
J	.05 [Min.]
K	1.00 ± .05
L	1.25 [Max.]
M	.05 ± .20
N	0° ~ 5°

NOTE: Each lead centerline is located within .25 mm of its true position [TP] at maximum material condition.



28-PIN PLASTIC SOP(330 mil)

ITEM	MILLIMETERS	INCHES
A	18.62 max.	.733 max.
B	1.194 max	.047 max
C	1.27 [TP]	.050 [TP]
D	.41 [Typ.]	.016 [Typ.]
E	.10 min.	.004 min.
F	2.85 max.	.110 max.
G	2.49 ± .13	.098 ± .005
H	11.81 ± .31	.465 ± .012
I	8.41 ± .13	.331 ± .005
J	1.70 ± .20	.067 ± .008
K	.25 [Typ.]	.010 [Typ.]
L	.91 ± .20	.036 ± .008

NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position [TP] at maximum material condition.

