

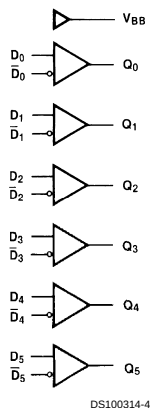
Low Power Hex ECL-to-TTL Translator

Features

- Pin/function compatible with 100125
- Meets 100125 AC specifications
- 50% power reduction of the 100125
- Differential inputs with built in offset
- Standard FAST® outputs
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Available to Microcircuit Drawing (SMD) 5962-9153101

When used in single-ended operation the apparent input threshold of the true inputs is 20 mV to 40 mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTI} power may be applied in either order.

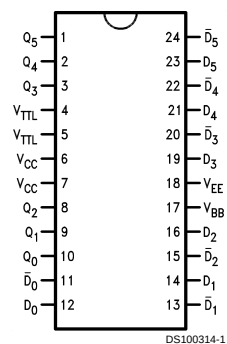
Pin Names	Description
D ₀ –D ₅	Data Inputs
$\overline{D}_0$ – $\overline{D}_5$	Inverting Data Inputs
Q ₀ –Q ₅	Data Outputs



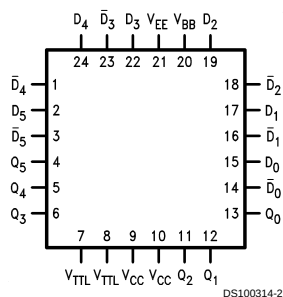
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Connection Diagrams

24-Pin DIP



24-Pin Quad Cerpak



Truth Table

Inputs		Outputs
D_n	$\bar{D}_n$	Q_n
L	H	L
H	L	H
L	L	L
H	H	L
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	-0.5V to +6.0V
Input Voltage (DC)	V_{EE} to +0.5V

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

-0.5V to V_{CC}

Current Applied to Output

in LOW State (Max)

twice the rated I_{OL} (mA)

ESD (Note 2)

≥2000V

Recommended Operating Conditions

Case Temperature (T_C)

Military

-55°C to +125°C

Supply Voltage (V_{EE})

-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$, $C_L = 50$ pF, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{BB}	Output Reference Voltage	-1380	-1260	mV	0°C to +125°C	$I_{V_{BB}} = -3 \mu A$, $V_{EE} = -4.2V$	(Notes 3, 4, 5)
		-1396	-1260		-55°C	$I_{V_{BB}} = -2.1$ mA	
						$V_{EE} = -5.7V$ $I_{V_{BB}} = -3$ mA	
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})	(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})	(Notes 3, 4, 5, 6)
V_{OH}	Output HIGH Voltage	2.5		mV	0°C to +125°C	$I_{OH} = -2.0$ mA	(Notes 3, 4, 5)
		2.4			-55°C		
V_{OL}	Output LOW Voltage		0.5	mV	-55°C to +125°C	$I_{OL} = 20$ mA	(Notes 3, 4, 5)
V_{DIFF}	Input Voltage Differential	150		mV	-55°C to +125°C	Required for Full Output Swing	(Notes 3, 4, 5)
V_{CM}	Common Mode Voltage	-2000	-500	mV	-55°C to +125°C		(Notes 3, 4, 5, 6)
I_{IH}	Input HIGH Current		350	μA	0°C to +125°C	$V_{IN} = V_{IH} (Max)$, $D_0-D_5 = V_{BB}$	(Notes 3, 4, 5)
			500		-55°C	$D_0-D_5 = V_{IL} (Min)$	
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{IN} = V_{IL} (Min)$, $D_0-D_5 = V_{BB}$	(Notes 3, 4, 5)
I_{OS}	Output Short Circuit Current	-150	-60	mA	-55°C to +125°C	$V_{OUT} = GND$ Test One Output at a Time	(Notes 3, 4, 5)
I_{CEX}	Output HIGH Leakage Current		250	μA	-55°C to +125°C	$V_{OUT} = 5.5V$	(Notes 3, 4, 5)
I_{EE}	V_{EE} Power Supply Current	-35	-12	mA	-55°C to +125°C	$D_0-D_5 = V_{BB}$	(Notes 3, 4, 5)
I_{TTL}	V_{TTL} Power Supply Current		65	mA	-55°C to +125°C	$D_0-D_5 = V_{BB}$	(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$; $V_{CC} = GND$; $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	1.50	5.00	1.60	4.70	1.70	5.70	ns	$C_L = 50$ pF	(Notes 7, 8, 9)
t_{PHL}	Data to Output								Figures 1, 3	

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ C$, temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Switching Waveform

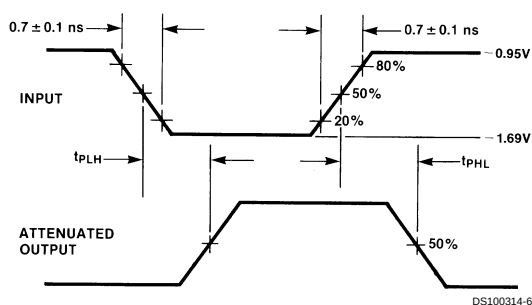
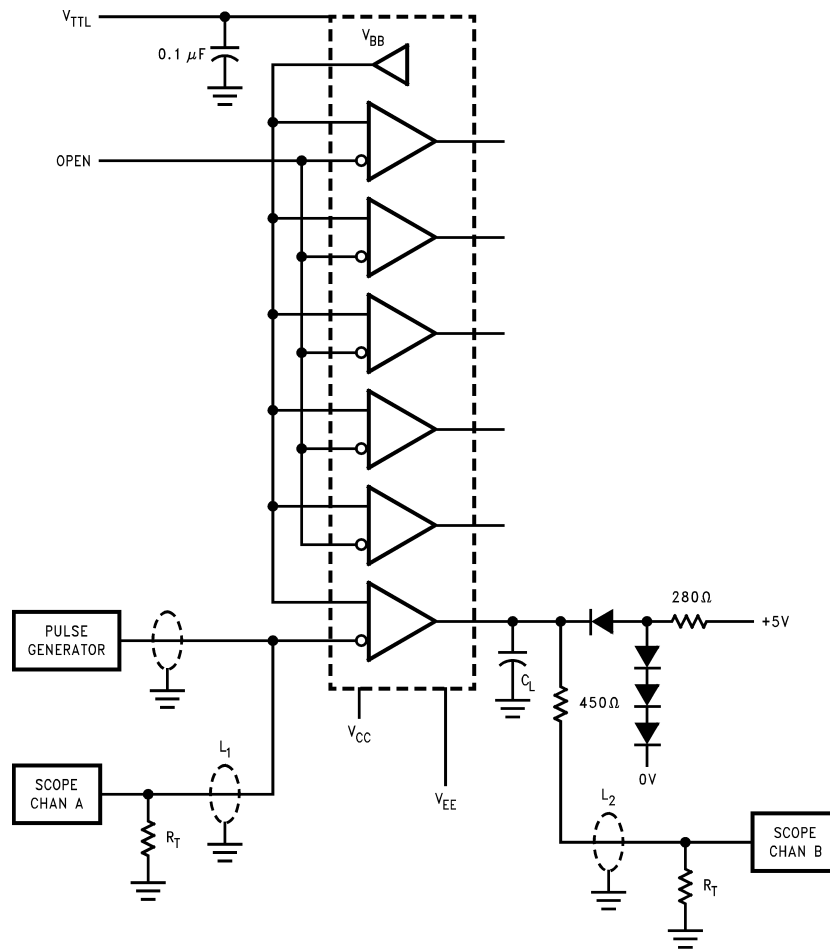


FIGURE 1. Propagation Delay

Test Circuits



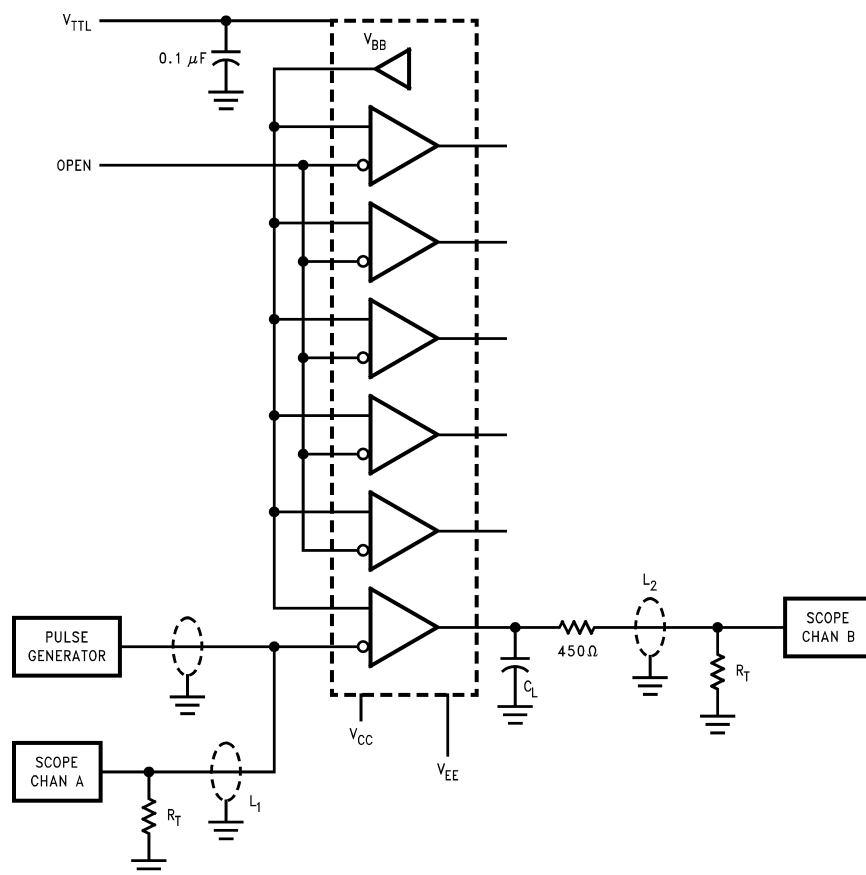
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Notes:

Notes:
 $V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\mu F$ from GND to V_{CC} , V_{EE} and V_{TTL}
 All unused outputs are loaded with 500Ω to GND
 C_L = Fixture and stray capacitance = 15 pF

FIGURE 2. AC Test Circuit for 15 pF Loading

Test Circuits (Continued)



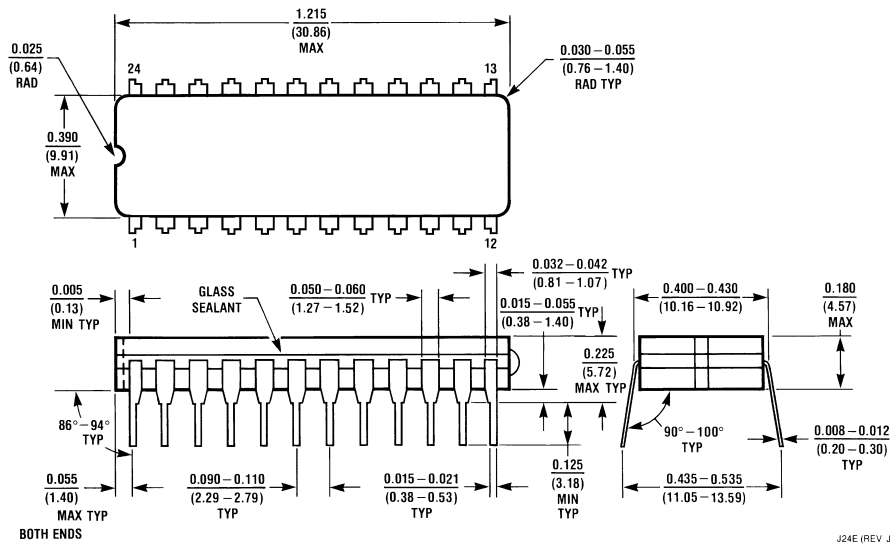
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Notes:

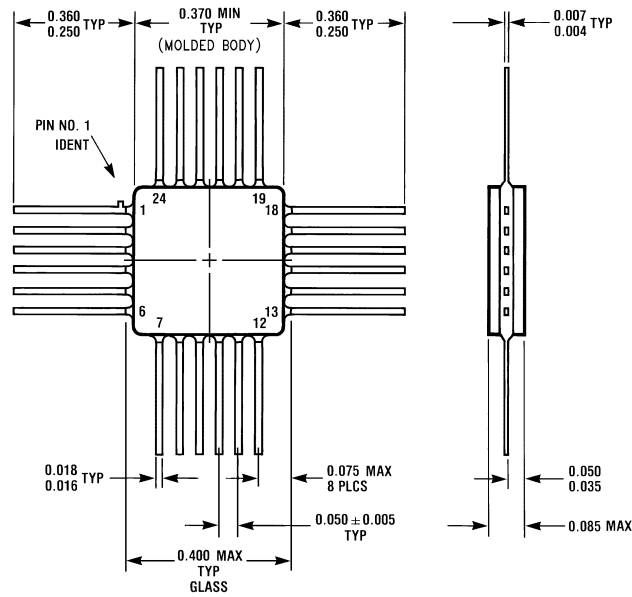
$V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$
 L_1 and L_2 = equal length 50 Ω impedance lines
 $R_T = 50 \Omega$ terminator internal to scope
 Decoupling 0.1 μF from GND to V_{CC} , V_{EE} and V_{TTL}
 All unused outputs are loaded with 500 Ω to GND
 C_L = Fixture and stray capacitance = 50 pF

FIGURE 3. AC Test Circuit for 50 pF Loading

Physical Dimensions inches (millimeters) unless otherwise noted



24 Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24 Lead Quad Cerpak (F)
NS Package Number W24B

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179