

NTE5491 thru NTE5496 Silicon Controlled Rectifier (SCR) 10 Amp

Description:

The NTE5491 through NTE5496 are silicon controlled rectifiers designed primarily for half-wave AC control applications such as motor controls, heating controls, power supplies, or wherever half-wave silicon gate-controlled, solid-state devices are needed.

Features:

- Glass-Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 600 Volts

Absolute Maximum Ratings: ($T_J = +125^{\circ}\text{C}$ unless otherwise specified)

Peak Repetitive Off-State Blocking Voltage, V_{RRM} , V_{DRM}	
NTE5491	100V
NTE5492	200V
NTE5494	400V
NTE5496	600V
Peak Non-Repetitive Reverse Voltage, V_{RSM}	
NTE5491	150V
NTE5492	300V
NTE5494	500V
NTE5496	720V
RMS On-State Current (All Conduction Angles), $I_{T(RMS)}$	25A
Average On-State Current ($T_C = +65^{\circ}\text{C}$), $I_{T(AV)}$	16A
Peak Non-Repetitive Surge Current, I_{TSM}	
(One cycle, 60Hz, Preceeded and followed by rated Current and Voltage)	150A
Circuit Fusing Considerations ($T_J = -40^{\circ}$ to $+125^{\circ}\text{C}$, $t = 1$ to 8.3ms), I^2t	93A ² s
Peak Gate Power Dissipation, P_{GM}	5W
Average Gate Power Dissipation, $P_{G(AV)}$	500mW
Peak Forward Gate Current, I_{GT}	
NTE5491, NTE5492, NTE5494	2.0A
NTE5496	1.2A
Operating Junction Temperature Range, T_J	-65° to $+125^{\circ}\text{C}$
Storage Temperature Range, T_{stg}	-65° to $+150^{\circ}\text{C}$
Typical Thermal Resistance, Junction-to-Case, R_{thJC}	2 $^{\circ}\text{C/W}$
Stud Torque	30 in.lb.

Electrical Characteristics: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Forward Blocking Current NTE5491	$I_{D(AV)}$	Rated V_{DRM} , Gate Open $T_J = +125^\circ\text{C}$	–	–	6.5	mA
NTE5492			–	–	6.0	mA
NTE5494			–	–	4.0	mA
NTE5496			–	–	2.5	mA
Average Reverse Blocking Current NTE5491	$I_{R(AV)}$	Rated V_{RRM} , Gate Open $T_J = +125^\circ\text{C}$	–	–	6.5	mA
NTE5492			–	–	6.0	mA
NTE5494			–	–	4.0	mA
NTE5496			–	–	2.5	mA
Peak Forward Blocking Current	I_{DRM}	Rated V_{DRM} , Gate Open	–	–	10	μA
Peak Reverse Blocking Current	I_{RRM}	Rated V_{RRM} , Gate Open, $T_J = +125^\circ\text{C}$	–	–	20	mA
Peak On–State Voltage	V_{TM}	$I_{TM} = 50.3\text{A}$ Peak, Note 1	–	–	2	V
DC Gate–Trigger Current	I_{GT}	$V_{AK} = 12\text{VDC}$, $R_L = 50\Omega$	–	–	40	mA
DC Gate–Trigger Voltage	V_{GT}	$V_{AK} = 12\text{VDC}$, $R_L = 50\Omega$	–	0.65	2.0	V
Gate Non–Trigger Voltage	V_{GD}	Rated V_{DRM} , $R_L = 50\Omega$, $T_J = +125^\circ\text{C}$	0.25	–	–	V
DC Holding Current	I_H	$V_{AK} = 12\text{V}$, Gate Open	–	7.3	50	mA
Critical Rate–of–Rise of Off–State Voltage	dv/dt	Rated V_{DRM} , Exponential Waveform, $T_C = +125^\circ\text{C}$, Gate Open	–	30	–	$\text{V}/\mu\text{s}$

Note 1. Pulse Test: Pulse Width $\leq 1\text{ms}$, Duty Cycle $\leq 2\%$.

