

576-BIT BIPOLAR RAM (64×9)

82S09/82S19 (O.C.)

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (-55°C to +125°C) specify S82S09/19 I, R or F.

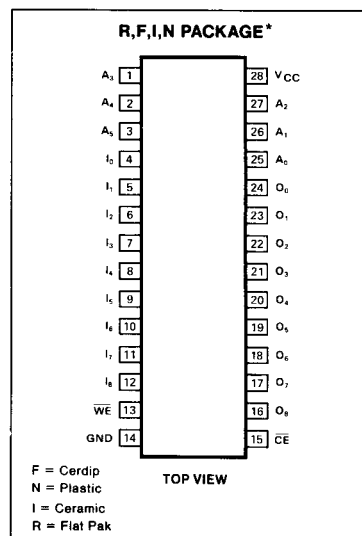
FEATURES

- Address access time:
N82S09: 45ns max
S82S09: 80ns max
N82S19: 35ns max
S82S19: 60ns max
- Write cycle time:
N82S09/19: 45ns max
S82S09: 80ns max
S82S19: 70ns max
- Power dissipation: 1.3mW/bit typ
- Input loading:
N82S09/19: -100μA max
S82S09/19: -150μA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- 82S09 Output is Non-Blanked During Write
- 82S19 Output is Blanked During Write

APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATION

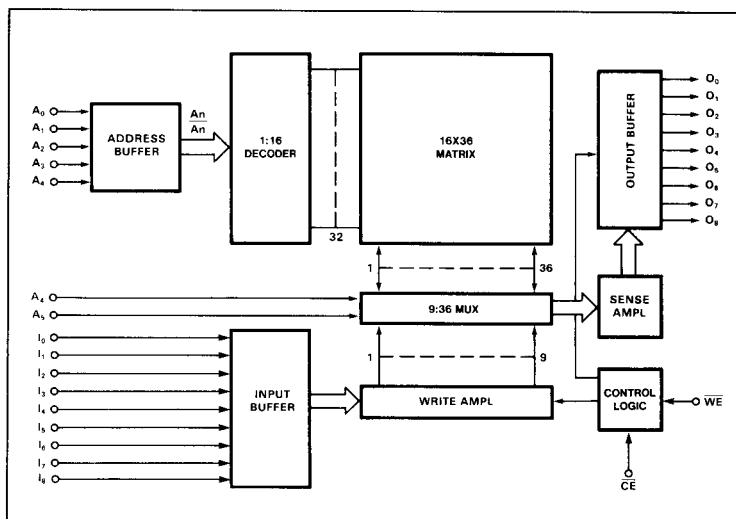


TRUTH TABLE

MODE	CE	WE	IN	ON	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	V _{dc}
V _{IN}	Input voltage	+5.5	V _{dc}
	Output voltage		V _{dc}
V _{OH}	High	+5.5	
T _A	Temperature range		°C
	Operating		
	N82S09/19	0 to +75	
	S82S09/19	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS^{1,7}N82S09/19: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25VS82S09/19: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER ¹	TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL}	Input voltage							V
V _{IH}	Low			.85	2.2		.80	
V _{IC}	High							
	Clamp ²			-1.5			-1.5	
V _{OL}	Output voltage							V
	Low ³			0.5			0.5	
I _{IL}	Input current							μA
I _{IH}	Low			-100			-150	
	High			25			40	
I _{OLK}	Output current							μA
	Leakage ⁴			40			60	
I _{CC}	V _{CC} supply current ⁵			190			200	mA
C _{IN}	Capacitance							pF
C _{OUT}	Input		5			5		
	Output		8			8		

Refer to notes on next page.

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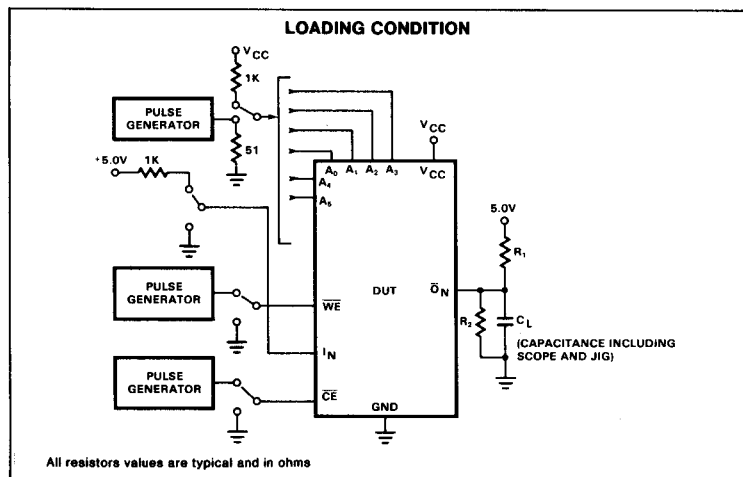
AC ELECTRICAL CHARACTERISTICS⁷R₁ = 600Ω, R₂ = 900Ω, C_L = 30pF, for 82S09R₁ = 510Ω, R₂ = 750Ω, C_L = 30pF, for 82S19N82S19: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25VS82S19: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T _{AA}	Access time				45			80			35			60	ns
T _{CE}	Chip enable				30			50			25			40	ns
T _{CD}	Disable time	Output			30			50			25			35	ns
T _{WD}	Valid time	Output			50			80			25			50	ns
T _{WR}	Write recovery time	Output									25			50	ns
T _{WSA}	Setup and hold time	Write enable	5	5		10			5			10			ns
T _{WHA}	Setup time														
T _{WHD}	Hold time														
T _{WSD}	Setup time														
T _{WHD}	Hold time	Write enable	35	5		50	5		30	5		45	5		
T _{WSC}	Setup time	Write enable	5	5		10			5			10			ns
T _{WHC}	Hold time														
T _{WP}	Pulse width		35			50			35			50			ns
	Write enable ⁶														

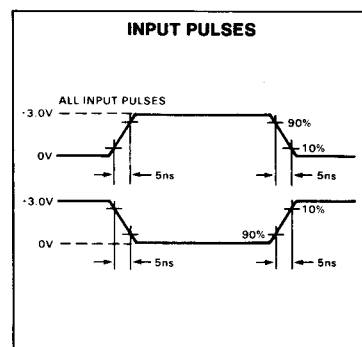
NOTES

1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT



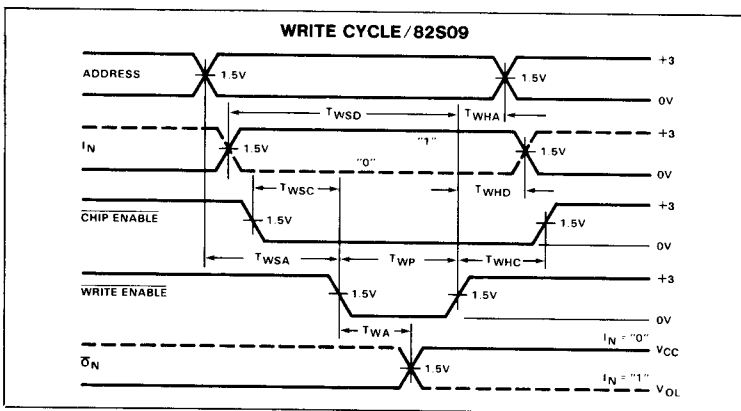
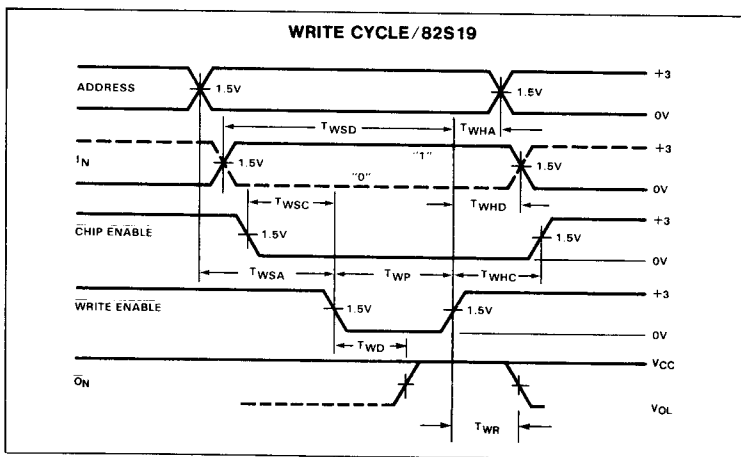
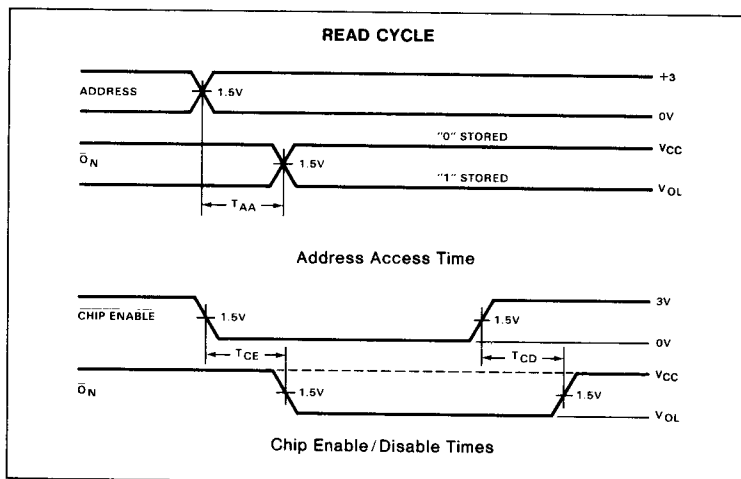
VOLTAGE WAVEFORM



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TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD}** Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA}** Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC}** Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD}** Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP}** Width of Write Enable pulse.
- T_{WSA}** Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD}** Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD}** Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
- T_{WHC}** Required delay between end of Write Enable pulse and end of Chip Enable.
- T_{WHA}** Required delay between end of Write Enable pulse and end of valid Address.
- T_{WR}** Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
- T_{WA}** Delay between beginning of Write Enable pulse and when data output reflects complement of data input.