

FEATURES

- Two independently-powered 622.08MHz clock sources one chip
- Differential PECL outputs
- TTL/CMOS compatible inputs
- SONET compliant jitter performance ($\leq 0.01\text{UI}$)
- Choice of three reference frequencies for each PLL
- Only 395mW per PLL (typ)
- Complies with Bellcore, CCITT and ANSI standards
- Single +5 volt power supply
- Fully compatible with industry standard 10KH I/O levels
- Available in 28-pin PLCC package

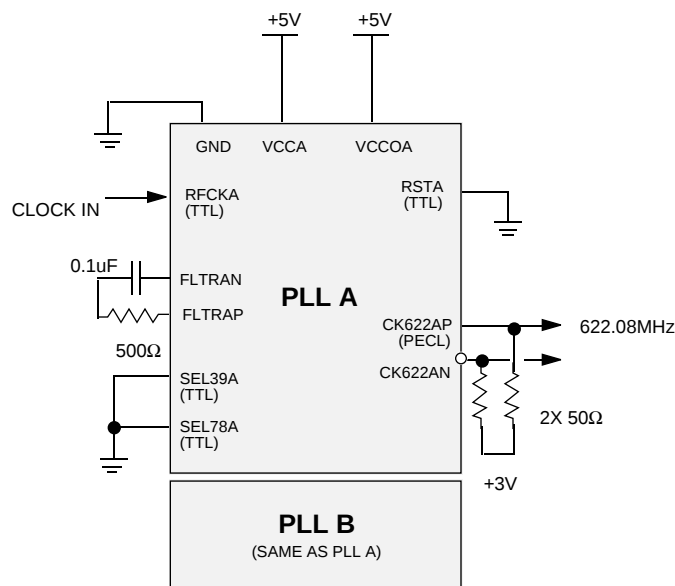
DESCRIPTION

Micrel-Synergy's SY89425 Dual Phase Locked Loop (PLL) consists of two totally separate, SONET compliant 622.08MHz clock generators on one chip. The user may select to power both PLLs or PLL A only. Each PLL produces a low-jitter OC-12/STS-12 clock rate from an input reference clock of 38.88, 51.84, or 77.76MHz. When using both PLLs, it is not necessary that they share a common reference clock (e.g., PLL A may operate from an STS-1 reference of 51.84MHz, while PLL B operates from an OC-3/STS-3 reference of 77.76MHz).

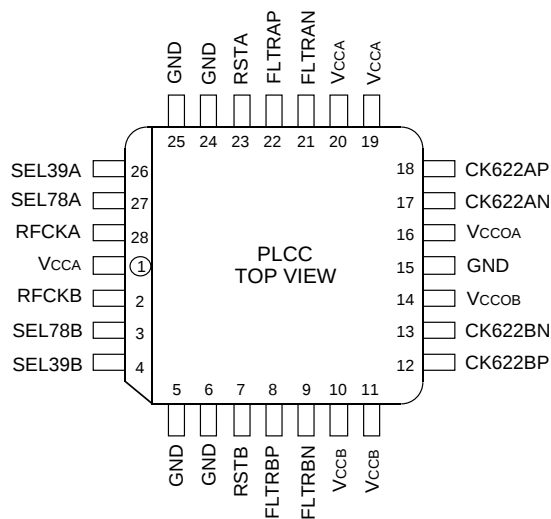
The SY89425 operates from a single +5 volt supply, and requires only a simple series RC loop filter for each PLL.

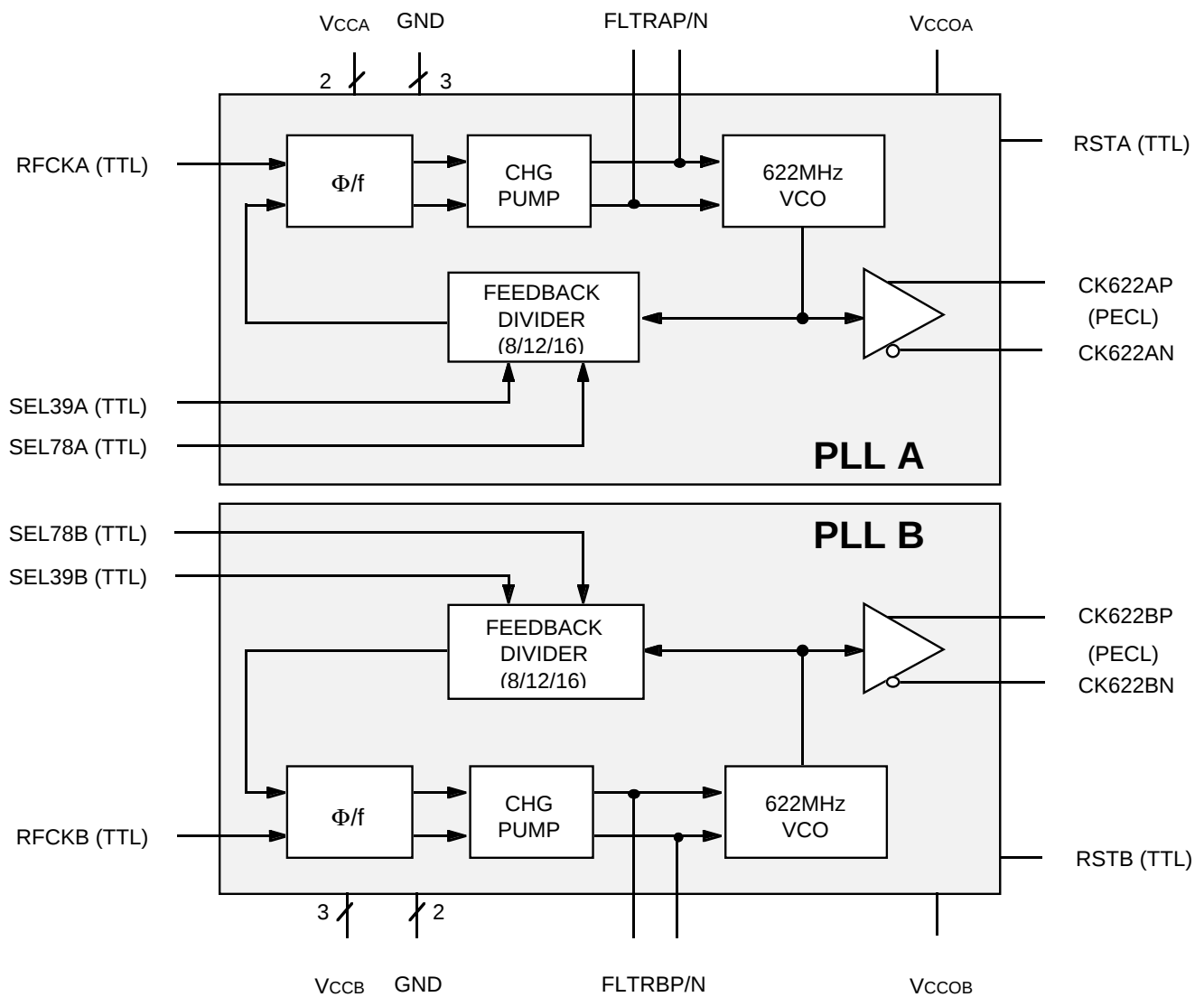
Coupling Micrel-Synergy's advanced PLL technology with our proprietary ASSET™ bipolar process has produced a clock generator IC which exceeds applicable Bellcore and ANSI specifications, while setting a new standard for performance and flexibility.

TYPICAL APPLICATION



PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION**INPUTS****RFCKB [Reference Clock B] TTL**

Reference clock in for PLL B. (38.88, 51.84 or 77.76MHz).

SEL39B [38.88MHz Select B] TTL

Logic HIGH on this pin denotes a 38.88MHz input reference clock for PLL B. Tie to logic LOW if input is not 38.88MHz.

SEL78B [77.76MHz Select B] TTL

Logic HIGH on this pin denotes a 77.76MHz input reference clock for PLL A. Tie to logic LOW if input is not 77.76MHz.

RSTB [Reset B] TTL

Tie to logic LOW for normal operation; logic HIGH forces reset of internal Phase Detector & feedback dividers on PLL B.

FLTRBP, FLTRBN (Loop Filter B, Pos & Neg) Analog.

Connect a series RC loop filter between these pins. The suggested loop filter is 0.1μF and 500 ohms, as shown in the typical application on page 3-9.

RSTA (Reset A) TTL

Tie to logic LOW for normal operation; logic HIGH forces reset of internal Phase Detector & feedback dividers on PLL A.

SEL78A [77.76MHz Select A] TTL

Logic HIGH on this pin denotes a 77.76MHz input reference clock for PLL A. Tie to logic LOW if input is not 77.76MHz.

SEL39A [38.88MHz Select A] TTL

Logic HIGH on this pin denotes a 38.88MHz input reference clock for PLL A. Tie to logic LOW if input is not 38.88MHz.

REFCKA [Reference Clock A] TTL

Reference clock in for PLL A.

FLTRAP, FLTRAN (Loop Filter A, Pos & Neg) Analog.

Connect a series RC loop filter between these pins. The suggested loop filter is 0.1μF and 500 ohms, as shown in the typical application on page 5-527.

OUTPUTS

CK622BP, CK622BN (Clock Out B) Differential PECL 622.08MHz output clock from PLL B.

CK622AP, CK622AN (Clock Out A) Differential PECL 622.08MHz output clock from PLL A.

POWER & GROUND

VCCA +5V for PLL A.

VCCB +5V for PLL B.

VCCOA +5V for PLL A PECL outputs.

VCCOB +5V for PLL B PECL outputs.

GND Ground (0 volts)

REFERENCE FREQUENCY SELECTION

SEL39	SEL78	f _{RFCK}
0	0	51.84
0	1	77.76
1	0	38.88
1	1	77.76

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{CC}	Power Supply	0 to +7	V
V _I	Input Voltage	0 to V _{CC}	V
I _{OUT}	Output Current —Continuous —Surge	50 100	mA
T _A	Operating Temperature Range	0 to +85	°C
T _{store}	Storage Temperature Range	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

PECL DC ELECTRICAL CHARACTERISTIC^{(1), (2)}

$V_{CCA} = V_{CCB} = V_{CCOA} = V_{CCOB} = +5V \pm 5\%$; $GND = 0V$; $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} - 1130$	$V_{CC} - 840$	$V_{CC} - 1070$	$V_{CC} - 790$	$V_{CC} - 1030$	$V_{CC} - 760$	$V_{CC} - 960$	$V_{CC} - 670$	mV
V_{OL}	Output LOW Voltage	$V_{CC} - 2000$	$V_{CC} - 1600$	$V_{CC} - 2000$	$V_{CC} - 1580$	$V_{CC} - 2000$	$V_{CC} - 1580$	$V_{CC} - 2000$	$V_{CC} - 1545$	mV
V_{IH}	Input HIGH Voltage ⁽¹⁾	$V_{CC} - 1230$	$V_{CC} - 890$	$V_{CC} - 1170$	$V_{CC} - 840$	$V_{CC} - 1130$	$V_{CC} - 810$	$V_{CC} - 1060$	$V_{CC} - 720$	mV
V_{IL}	Input LOW Voltage ⁽¹⁾	$V_{CC} - 1950$	$V_{CC} - 1500$	$V_{CC} - 1950$	$V_{CC} - 1480$	$V_{CC} - 1950$	$V_{CC} - 1480$	$V_{CC} - 1950$	$V_{CC} - 1445$	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	μA

NOTES:

1. Forcing one input at a time. Apply V_{IH} (Max) or V_{IL} (Min) to all other inputs.
2. Airflow greater than 500lfpm is maintained.

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CCA} = V_{CCB} = V_{CCOA} = V_{CCOB} = +5V \pm 5\%$; $GND = 0V$; $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	$I_{OH} = -2mA$
V_{OL}	Output LOW Voltage	—	0.5	V	$I_{OL} = 4mA$
I_{OS}	Output Short Circuit Current	-150	-60	mA	$V_{OUT} = 0V$
V_{IH}	Input HIGH Voltage	2.0	—	—	—
V_{IL}	Input LOW Voltage	—	0.8	V	—

DC ELECTRICAL CHARACTERISTICS^{(1), (2), (3)}

$V_{CCA} = V_{CCB} = V_{CCOA} = V_{CCOB} = +5V \pm 5\%$; $GND = 0V$; $T_A = 0^\circ C$ to $85^\circ C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{EE}	Internal Operating Current	—	157	204	mA	Both PLLs powered
I_{OUT}	Termination Output Current	—	11	—	mA	50Ω to $V_{CC} - 2$, 50% duty cycle

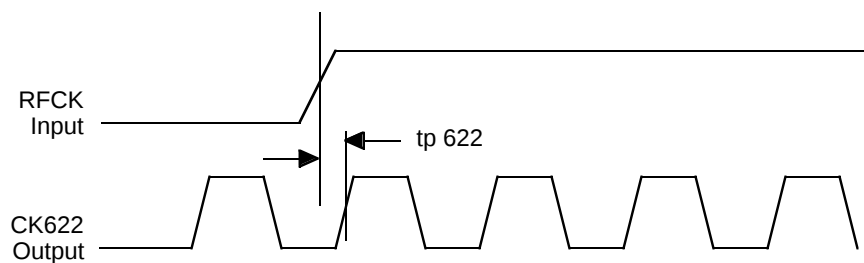
NOTES:

1. To calculate total power supply current into the V_{CC} pins: $I_{CC} = (n * I_{OUT})$; where n = number of ECL output pins used (ie, terminated).
2. To calculate total device power dissipation; $P_D = [I_{EE} * (V_{CC} - V_{EE})] + [n * I_{OUT} * 1.33]^{(3)}$.
3. Average ECL output voltage is calculated as $V_{OAVG} = (V_{OH(MAX)} + V_{OH(MIN)} + V_{OL(MAX)} + V_{OL(MIN)}) / 4 = 1.33V$.

AC ELECTRICAL CHARACTERISTICS

VCCA = VCCB = VCCOA = VCCOB = +5V ±5%; GND = 0V; TA = 0°C to 85°C

Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency	622.08 ±1%			MHz	Nominal
Reference Clock (RFCK) Frequency Tolerance	—	±20	—	ppm	77.76MHz
	—	±20	—	ppm	51.84MHz
	—	±10	—	ppm	38.88MHz
Reference Clock (RFCK) Input Duty Cycle	45	—	55	% of UI	
Acquisition Lock Time	—	—	15	μsec	
TTL Output Rise/Fall Time	—	—	2	ns	10% to 90% of amplitude, 15pF load
PECL Output Rise/Fall Time	—	—	500	ps	10% to 90%, 50Ω load, 5pF cap
CK622 Output Duty Cycle	45	—	55	% of UI	
tRST – RST pulse width	1	—	—	μsec	
tp622 Static Phase Offset of CK622	—	–0.7	—	ns	

TIMING WAVEFORMS

JITTER GENERATION

Jitter Generation Definition

Bellcore TR-NWT-000499 (Issue 4), section 7.3.3 "Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the absence of applied input jitter."

Jitter Generation Requirement

Bellcore TA-NWT-000253 (Issue 2), section 5.6.5.2 "For Category II interfaces, jitter generation shall not exceed 0.01 UI rms. For OC-N and STSX-N interfaces, a high-pass measurement filter with a 12kHz cutoff frequency shall be used." The low-pass cutoff frequency of the measurement filter shall be higher than 5MHz.

The characteristic of the measurement filter is shown below.

**SONET OC-12 Category II Jitter Generation Measurement
Filter Characteristics**

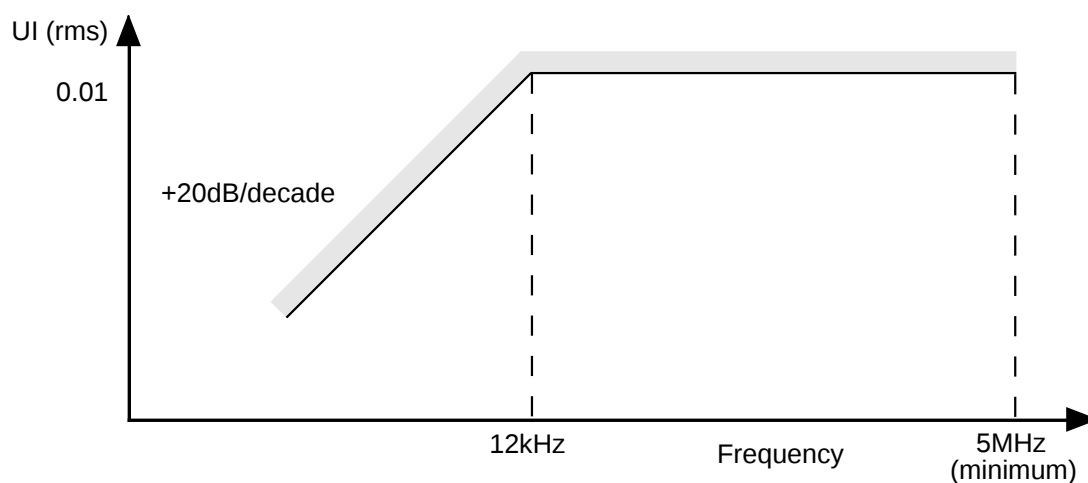
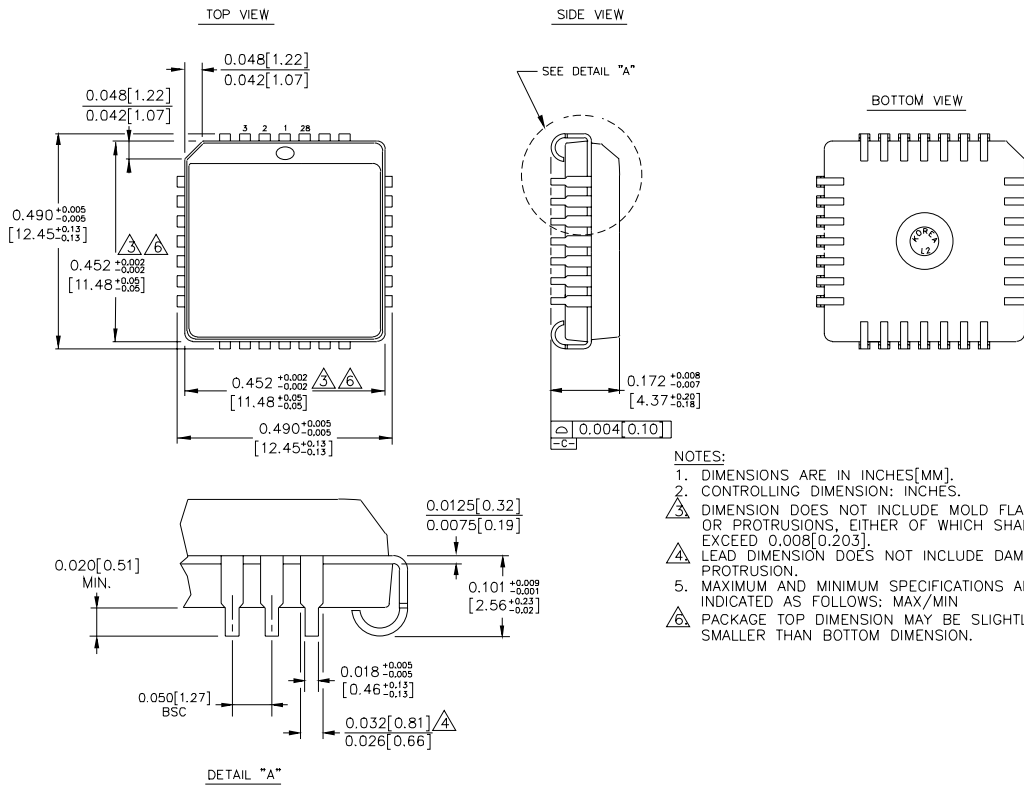


Figure 1

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89425JC	J28-1	Commercial
SY89425JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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