intel

ADVANCE INFORMATION

8XC196KR/KQ/JR/JQ
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KR/KQ/JR/JQ—16 Kbytes of On-Chip OTPROM
80C196KR/KQ/JR/JQ—ROMless

- High Performance CHMOS 16-Bit CPU
- 16 MHz Operating Frequency
- Up to 488 Bytes of On-Chip Register RAM
- 256 Bytes of Additional RAM (Code or Data RAM)
- Register-Register Architecture
- 8 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port (SIO) and Full Duplex Synchronous Serial I/O Port (SSIO) with Dedicated Baud Rate Generators
- Interprocessor Communication Slave Port
- Watchdog Timer
- High-Speed Peripheral Transaction Server (PTS)
- Two Programmable 16-Bit Timer/Counters with Prescale, Cascading, Standard and Quadrature Counting Inputs
- 10 High-Speed Capture/Compare (EPA)
- Two Dedicated High Speed Compare Registers
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus
- Programmable Bus (HOLD/HLDA)
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- Extended Temperature Available
- 68-Pin and 52-Pin PLCC Packages

Device	Pins/Package	OTPROM	Reg RAM	Internal RAM	I/O	EPA	SIO	SSIO	A/D
87C196KR	68 p PLCC	16K	512	256	56	10	Y	Y	8
87C196KQ	68 p PLCC	12K	384	128	56	10	Y	Y	8
87C196JR	52 p PLCC	16K	512	256	41	6	Y	Y	6
87C196JQ	52 p PLCC	12K	384	128	41	6	Y	Y	6
80C196KR	68 p PLCC	0	512	256	56	10	Y	Y	8
80C196KQ	68 p PLCC	0	384	128	56	10	Y	Y	8
80C196JR	52 p PLCC	0	512	256	41	6	Y	Y	6
80C196JQ	52 p PLCC	0	384	128	41	6	Y	Y	6

The 87C196KR/KQ/JR/JQ devices represent the 4th generation of MCS® 96 products implemented on Intel's advanced 1 micron process technology. These products are members of the 80C196 family of devices and the instruction set is the same as that of the 80C196KC. The 87C196JR is a 52-lead version of the 87C196KR device, while the 87C196KQ/JQ are memory scalars of the 87C196KR/JR.

The MCS 96 microcontroller family members are all high-performance microcontrollers with a 16-bit CPU. The 87C196KR is composed of the high-speed (16 MHz) core as well as the following peripherals: up to 16 Kbytes of on-chip EPROM, up to 512 bytes of Register RAM, 256 bytes of Code RAM, an eight-channel 10-bit analog to digital converter, an (8096 compatible) asynchronous/synchronous serial I/O port, an additional synchronous serial I/O port, 10 modularized multiplexed capture and compare channels (called the Event Processor Array), a sophisticated prioritized interrupt structure with the programmable Peripheral Transaction Server (PTS).

Additional register space is allocated for the EPA and can be windowed into the lower Register RAM area.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (**Express**) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the prefix identification for extended temperature designators.

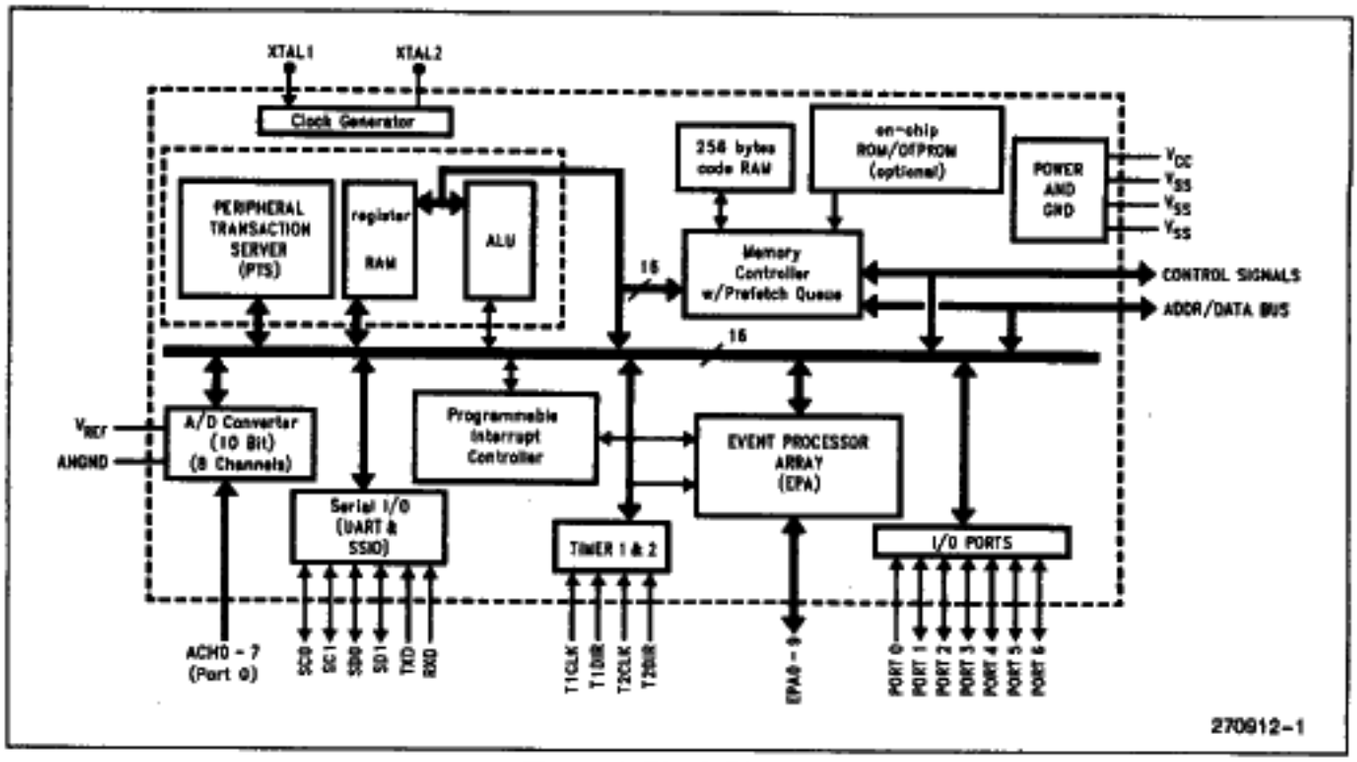


Figure 1. Block Diagram

0FFFFH 06000H	External Memory
05FFFH 02080H	Internal ROM/EPROM or External Memory
0207FH 0205EH	Reserved
0205DH 02040H	PTS Vectors
0203FH 02030H	Interrupt Vectors (upper)
0202FH 02020H	ROM/EPROM Security Key
0201FH	Reserved
0201BH	Reserved (must contain 20H)
0201AH	CCB1
02019H	Reserved (must contain 20H)

02018H	CCB0
02017H 02014H	Reserved
02013H 02000H	Interrupt Vectors (lower)
01FFFH 01F00H	Internal SFRs
01EFFH 00500H	External Memory
004FFH 00400H	Internal RAM
003FFH 00200H	External Memory
001FFH 18H	Register File
17H 00H	CPU SFR's

NOTES:
1. Reserved memory locations must contain 0FFH unless noted.
2. Reserved SFR bit locations must contain 0H unless noted.
3. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

Process Information

The 8XC196KR/JR/KQ/JQ is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

Table 1. Prefix Identification

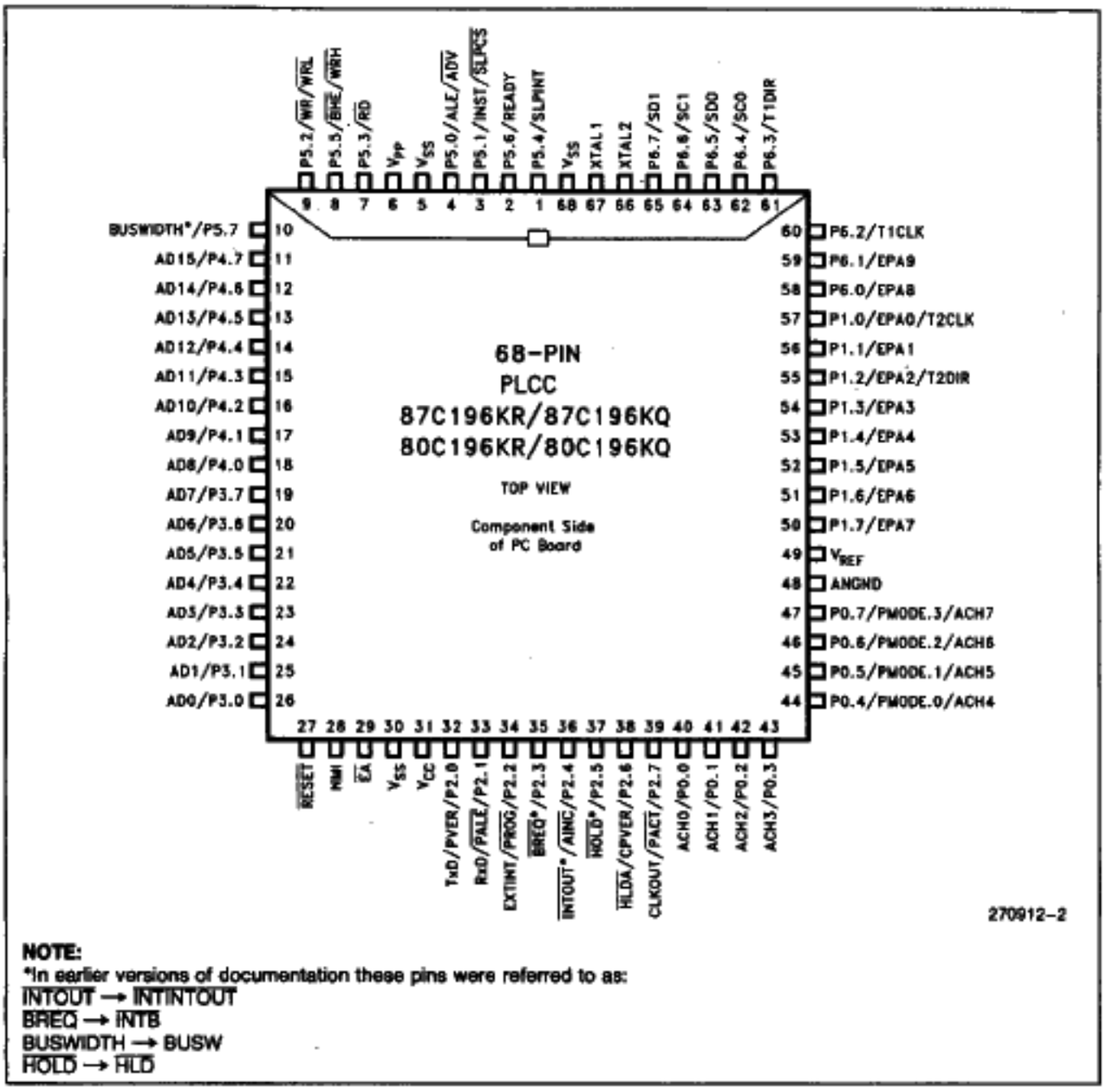
Device	Commercial PLCC	Express PLCC
80C196KR	N80C196KR	*TN80C196KR
80C196JR	N80C196JR	*TN80C196JR
80C196KQ	N80C196KQ	*TN80C196KQ
80C196JQ	N80C196JQ	*TN80C196JQ
87C196KR	N87C196KR	*TN87C196KR
87C196JR	N87C196JR	*TN87C196JR
87C196KQ	N87C196KQ	*TN87C196KQ
87C196JQ	N87C196JQ	*TN87C196JQ

*T = Extended Temperature, no burn-in.

Table 2. Thermal Characteristics

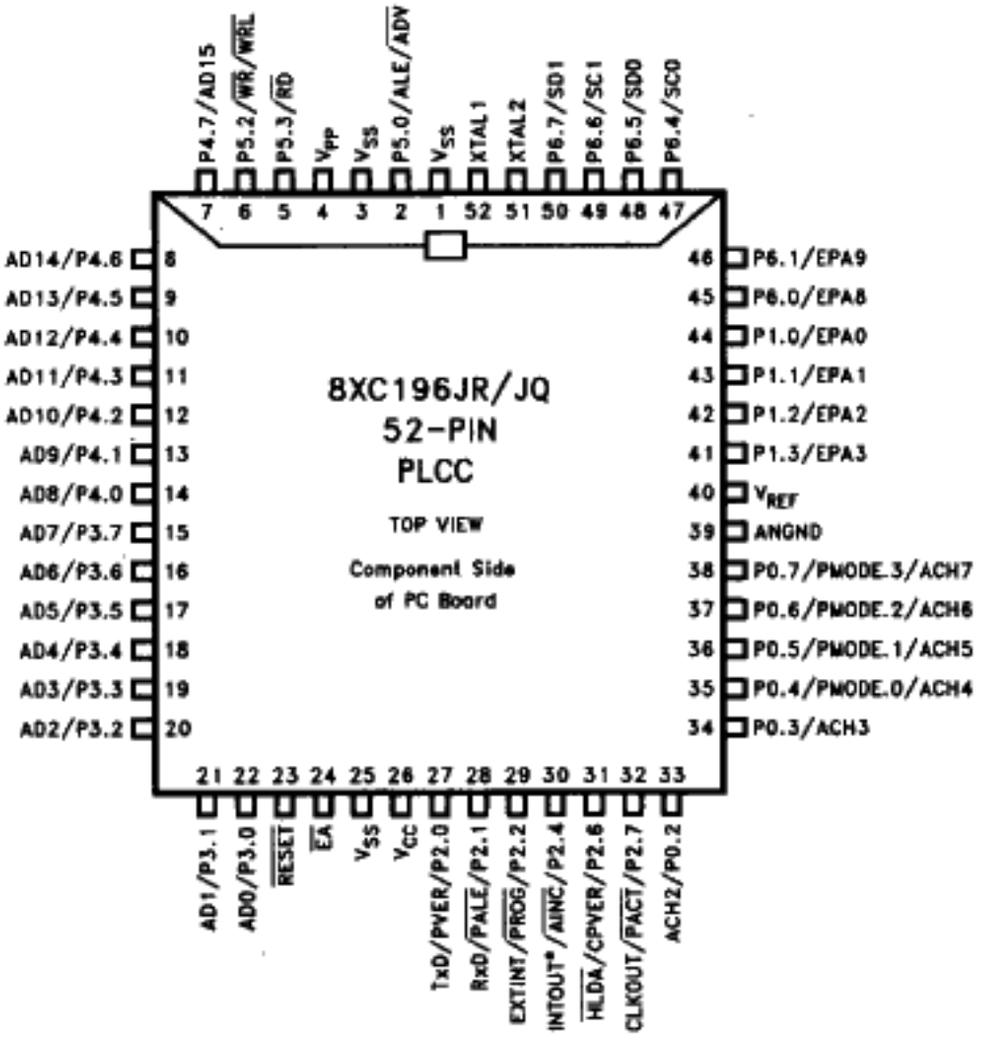
Package	θ_{ja}	θ_{jc}
52-Lead PLCC	35°C/W	12°C/W
68-Lead PLCC	35°C/W	13°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See Intel *Packaging Handbook*, (Order Number 240800) for a description of Intel's thermal impedance test methodology.



NOTE:
*In earlier versions of documentation these pins were referred to as:
INTOUT → INTINTOUT
BREQ → INTB
BUSWIDTH → BUSW
HOLD → HLD

Figure 2. Package Diagrams



NOTE:
*In earlier versions of documentation these pins were referred to as:
$\overline{\text{INTOUT}}$ → $\overline{\text{INT}}$/$\overline{\text{INTOUT}}$
$\overline{\text{BREQ}}$ → $\overline{\text{INTB}}$
BUSWIDTH → BUSW
$\overline{\text{HOLD}}$ → $\overline{\text{HLD}}$

Figure 2. Package Diagrams (Continued)

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the OTPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. If this function is not used, V_{PP} must be tied to V_{CC}.
ACH0–ACH7/PORT0	Analog inputs to the on-chip A/D converter.
$\overline{AINC}$	Input to automatically increment the address when in Programming mode.
ALE/$\overline{ADV}$/P5.0	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options allow a latch to demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. When the pin is ALE, the address can be latched on the falling edge. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE.
$\overline{BHE}$/$\overline{WRH}$/P5.5	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Can be used as standard I/O when not used as $\overline{BHE}$/$\overline{WRH}$.
$\overline{BREQ}$/P2.3	Bus Request output activated when the bus controller has a pending external memory cycle. Can be used as standard I/O when not used as $\overline{BREQ}$.
BUSWIDTH/P5.7	Input for bus width selection. If CCR bit 1 = 1 and CCR1 bit 2 = 1, this pin dynamically controls the Bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Can be used as standard I/O when not used as BUSWIDTH.
CLKOUT/P2.7	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Can be used as standard I/O when not used as CLKOUT.
CPVER	Cumulative Program Verify output. Indicates when all EPROM locations program correctly.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ = 1 causes memory accesses from locations 2000H to 5FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ = 0 causes all memory accesses to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
EPA0–7/PORT1 EPA8-9/P6.0–6.1	Event Processor Array pin for High Speed capture and compare. EPA0 and EPA2 also function as T2CLK and T2DIR. Can be used as standard I/O when not used as EPA or T2 clock functions.
EXTINT/P2.2	A positive transition on this pin causes a maskable interrupt vector through memory location 203CH. May be used as standard I/O if not used as EXTINT.
$\overline{HLDA}$/P2.6	Bus Hold Acknowledge output indicating release of the bus. Can be used as standard I/O when not used as $\overline{HLDA}$.
$\overline{HOLD}$/P2.5	Bus Hold input requesting control of the bus. Can be used as standard I/O when not used as $\overline{HOLD}$.

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PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
INST/P5.1	Output high during an external memory instruction fetch. INST is valid throughout the bus cycle. INST is low otherwise. Can be used as standard I/O when not used as INST.
$\overline{\text{INTOUT}}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Can be used as standard I/O if not used as $\overline{\text{INTOUT}}$.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
$\overline{\text{PACT}}$	Output that indicates when the device is currently programming itself. Not active during slave programming.
$\overline{\text{PALE}}$	Input to latch the address during programming modes.
PMODE.0–PMODE.3	Programming mode select inputs.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. These pins are also used as inputs by EPROM parts to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, $\overline{\text{BREQ}}$, $\overline{\text{INTOUT}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, CLKOUT).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/$\overline{\text{ADV}}$, INST, $\overline{\text{WR}}$/$\overline{\text{WRL}}$, $\overline{\text{RD}}$, SLPINT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
$\overline{\text{PROG}}$	Programming mode enable input.
PVER	Program Verify output. Goes high after a byte/word is programmed to indicate a successful operation.
$\overline{\text{RD}}$/P5.3	Read signal output to external memory. $\overline{\text{RD}}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{\text{RD}}$.
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 with the appropriate timings, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{\text{RESET}}$	Reset input to and output from the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O port. Can be used as standard I/O if not used as RXD.
$\overline{\text{SLPCS}}$	Slave port chip select input pin. Can be used as standard I/O if not used as $\overline{\text{SLPCS}}$.
SLPINT/P5.4	Slave Port Interrupt Output pin. Can be used as standard I/O when not used as SLPINT.
SSIO/P6.4–6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 serve as clock pins and SD0/SD1 are data pins. Can be used as standard I/O if not used for serial I/O.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
T1CLK/P6.2	TIMER1 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T1CLK.
T1DIR/P6.3	TIMER1 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T1DIR.
T2CLK/P1.0	TIMER2 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T2CLK.
T2DIR/P1.2	TIMER2 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T2DIR.
TXD/P2.0	Transmit data output pins for the Serial I/O port. Can be used as standard I/O if not used as TXD.
$\overline{WR}/\overline{WRL}$/P5.2	Write and Write Low output to external memory. $\overline{WR}$ will go low for every external write. $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}/\overline{WRL}$ is active only during external memory writes. Can be used as standard I/O when not used as $\overline{WR}/\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.

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ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... −60°C to +150°C

Ambient Temperature under Bias ..... −55°C to +125°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5V to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation 1.0W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz(4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

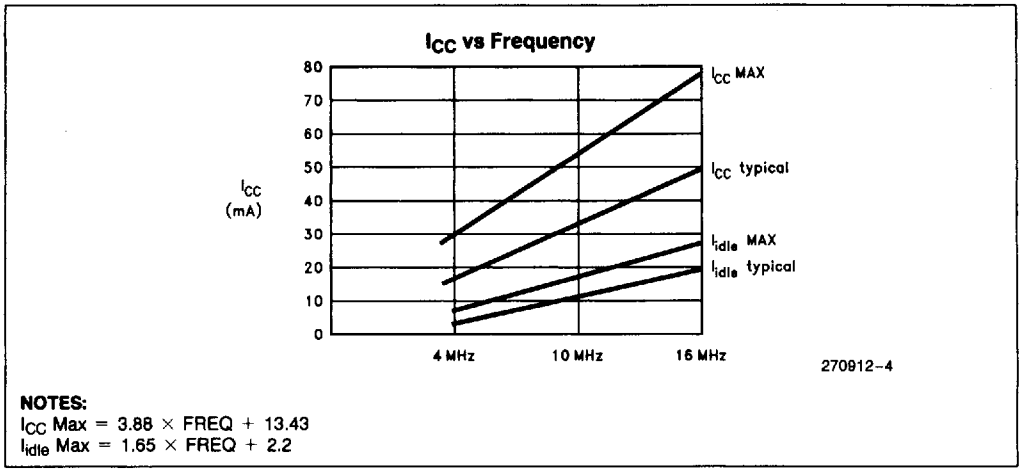
DC CHARACTERISTICS (Over Specified Operating Conditions)(9)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (All Pins)	−0.5V		0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Outputs Configured as Push/Pull)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA(3, 5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Push/Pull)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 µA(3, 5, 8) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OH2}	Output High Voltage in RESET	V_{CC} − 1V			V	I_{OH} = −15 µA(1, 7)
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(2)
I_{LI1}	Input Leakage Current (Port 0—A/D Inputs)		±1	±3	µA	$V_{SS} < V_{IN} < V_{REF}$
I_{IH}	Input High Current (NMI)			+175	µA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(10)

DC CHARACTERISTICS (Over Specified Operating Conditions)(9) (Continued)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		60	75	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While Device in Reset)
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	TBD	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance (Approx)		150K		Ω	(6)

NOTES:
1. All BD (Bidirectional) pins except INST and CLKOUT. BD pins include Port1, Port2, Port3, Port4, Port5 (as a port), and Port6.
2. Standard Input pins include XTAL1, $\overline{EA}$, $\overline{RESET}$, and Port 1/2/3/4/5/6 when setup as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. This specification applies to P3/4 only when used as an address bus supplying the address.
9. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
10. Worst case is at upper limit of test conditions.



NOTES:
I_{CC} Max = 3.88 × FREQ + 13.43
I_{idle} Max = 1.65 × FREQ + 2.2

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AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KR/KQ/JR/JQ:

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC}-75$	ns(2)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC}-70$	ns(2)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC}-30$	ns(1, 2)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC}-15$	$2T_{OSC}-40$	ns(1, 2)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC}-75$	ns(2)
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC}-60$	ns(2)
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns(2)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC}-55$	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC}-22$	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC}-50$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns

NOTE:
1. If max is exceeded, additional wait states will occur.
2. Does not apply to JR/JQ.

AC CHARACTERISTICS (Over Specified Operating Conditions)

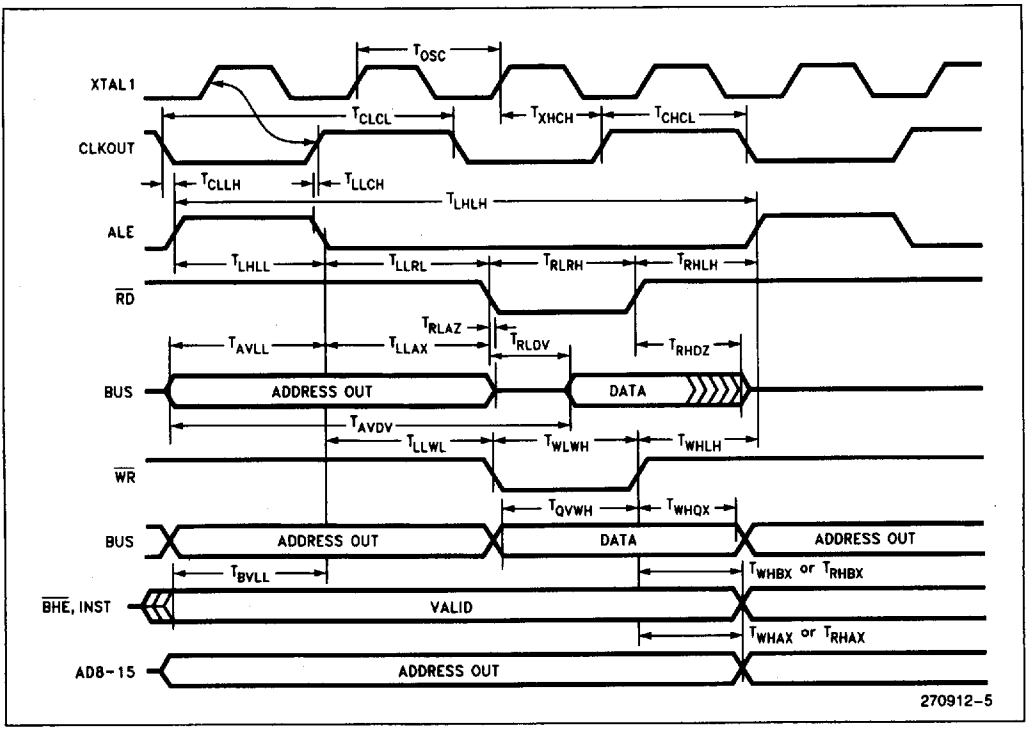
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KR/KQ/JR/JQ will meet these specifications.

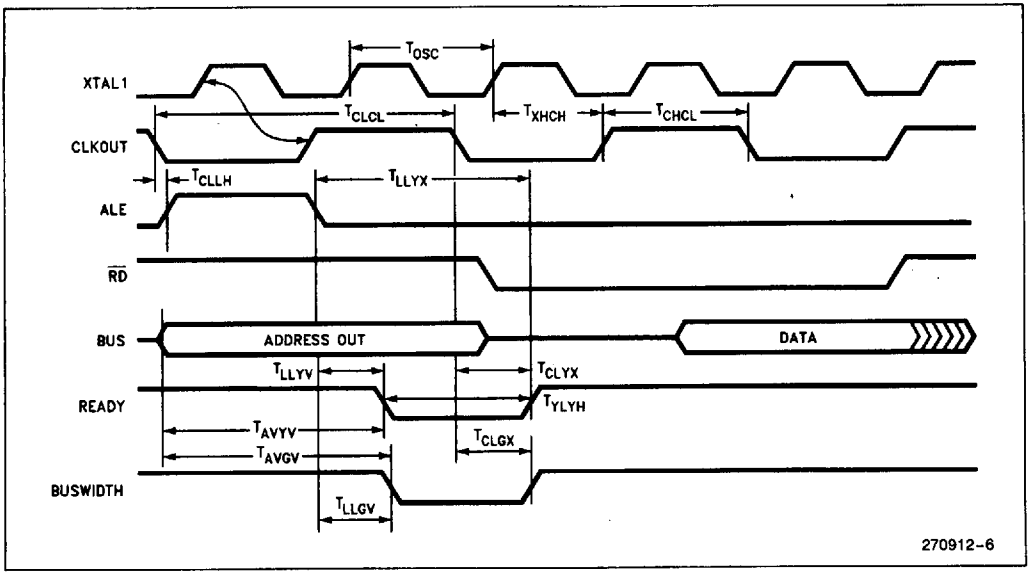
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	4.0	16.0	MHz(1)
T_{OSC}	Oscillator Period (1/Fxtal)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+15$	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Falling Edge to CLKOUT Rising	−20	15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns
T_{AVLL}	Address Setup to ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-15$		ns
T_{LLAX}	Address Hold after ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-40$		ns
T_{LLRL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-30$		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns(5)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	T_{OSC}	$T_{OSC}+25$	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	−5	25	ns
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-23$		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-30$		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-25$		ns
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	$T_{OSC}-10$	$T_{OSC}+15$	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{BVLL}	BHE Valid to ALE Falling Edge	$T_{OSC}-15$		ns(6)

NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.
6. Does not apply to JR/JQ.

System Bus Timing



Buswidth Timings



HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	65		ns	(1, 2)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	(2)
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	(2)
T_{AZHAL}	HLDA Low to Address Float		25	ns	(2)
T_{BZHAL}	HLDA Low to BHE, INST, RD, WR Weakly Driven		25	ns	(2)
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	(2)
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	(2)
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	(2)
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns	(2)
T_{CLLH}	CLKOUT Low to ALE High	−10	15	ns	

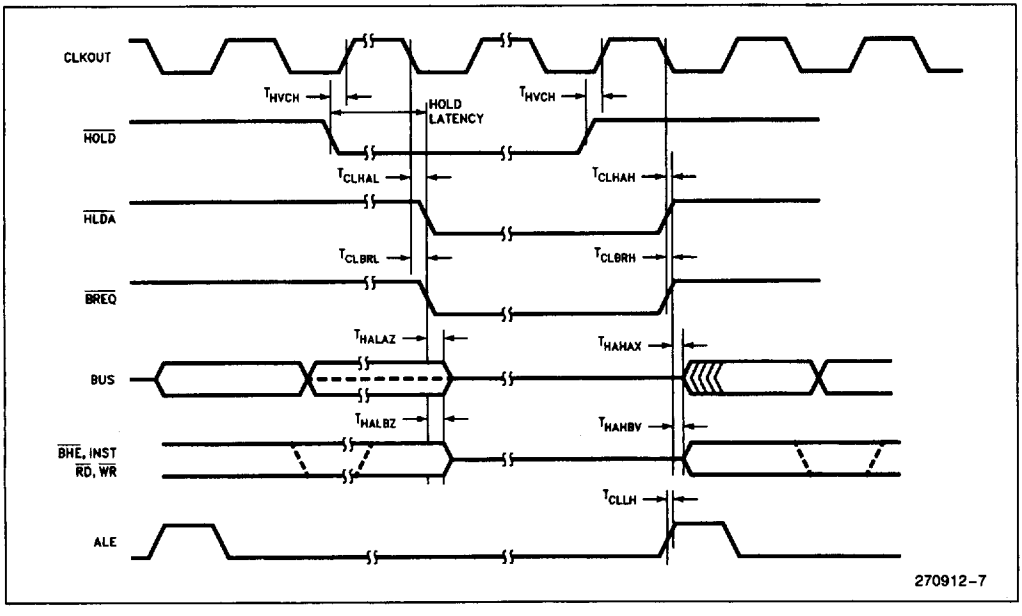
NOTE:
1. To guarantee recognition at next clock.
2. Does not apply to JR/JQ.

HOLD LATENCY

	Max
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

DC SPECIFICATIONS IN HOLD

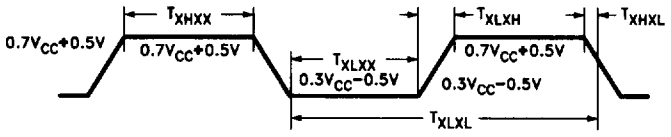
Parameter	Min	Max	Units
Weak Pullups on ADV, RD, WR, WRL, BHE	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4V



EXTERNAL CLOCK DRIVE

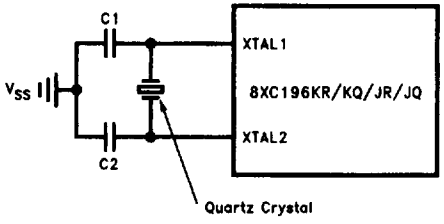
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4.0	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270912-8

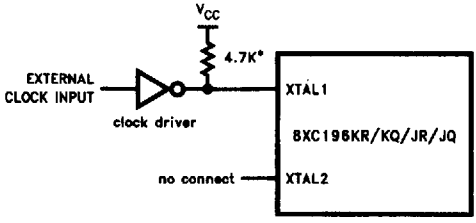
EXTERNAL CRYSTAL CONNECTIONS



270912-16

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using quartz crystals, typically C1 ≈ 22 pF and C2 ≈ 22 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

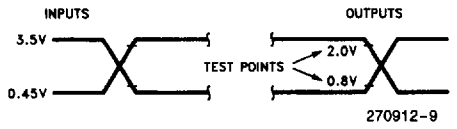
EXTERNAL CLOCK CONNECTIONS



270912-17

*Required if TTL driver used.
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



270912-9

NOTE:
AC Testing Inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS

270912-10

NOTE:
For Timing Purposes a Port Pin is no longer floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loading V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \leq 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
BR— $\overline{BREQ}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
Q— Data Out
R— $\overline{RD}$
W— $\overline{WR}$/$\overline{WRH}$/$\overline{WRI}$
X— XTAL1
Y— READY

4

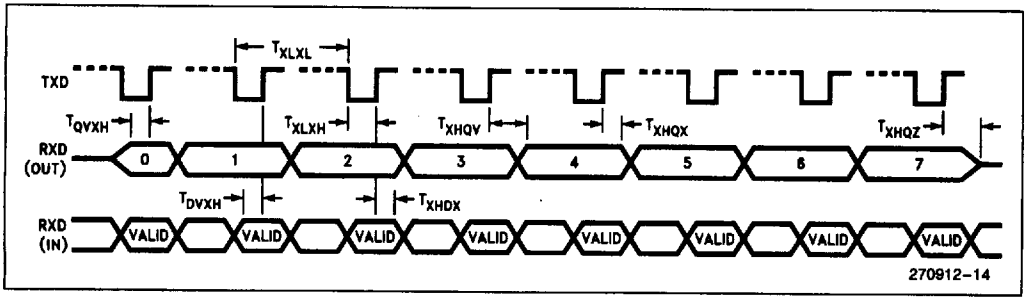
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT TIMING—SHIFT REGISTER MODE (Over Specified Operating Conditions)
Test Conditions: Load Capacitance = 100 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD_TIME special function register to the appropriate value. The AD_TIME register only programs the speed at which the conversions are performed, not the speed it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

A/D CONVERTER SPECIFICATION

After a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12V.

There is an AD_TEST register that allows for conversion on ANGND and V_{REF} as well as zero offset adjustment. The Absolute Error listed is WITHOUT doing any adjustments.

10-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		μs(3)
T_{CONV}	Conversion Time	16.5	19.5	μs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical (1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3	LSBs
Differential Non-Linearity		> −0.5	+0.5	LSBs
Channel-to-Channel Matching	±0.1	0	±1	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	1.2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V
Sampling Capacitor	2			pF
DC Input Leakage		0	±3	μA

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

8-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		μs(3)
T_{CONV}	Conversion Time	16.5	19.5	μs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

The 8-bit mode trades off resolution for a faster conversion time. The AD_TIME register must be used when performing an 8-bit conversion.

Parameter	Typ(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±2	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±2	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB(2, 3)	
Feedthrough	−60			dB(2)	
V_{CC} Power Supply Rejection	−60			dB(2)	
Input Series Resistance		750	1.2K	Ω	
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	
Sampling Capacitor	2			pF	
DC Input Leakage		0	±3	μA	

NOTES:
*An "LSB", as used here, has a value of approximately 20 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

OTPROM PROGRAMMING

OPERATING CONDITIONS DURING PROGRAMMING(3)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	$\overline{EA}$ Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).

AC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(1)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the word dump mode. For programming pulses use 100 μs.

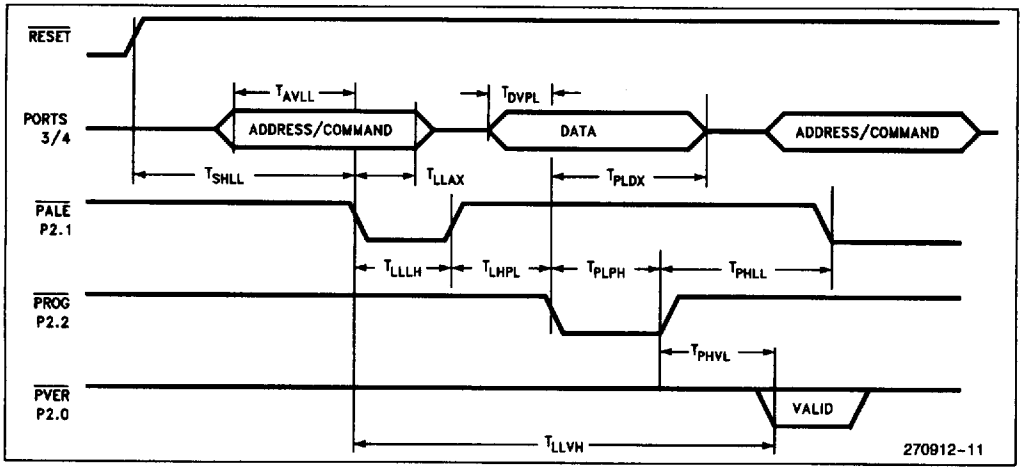
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100	mA

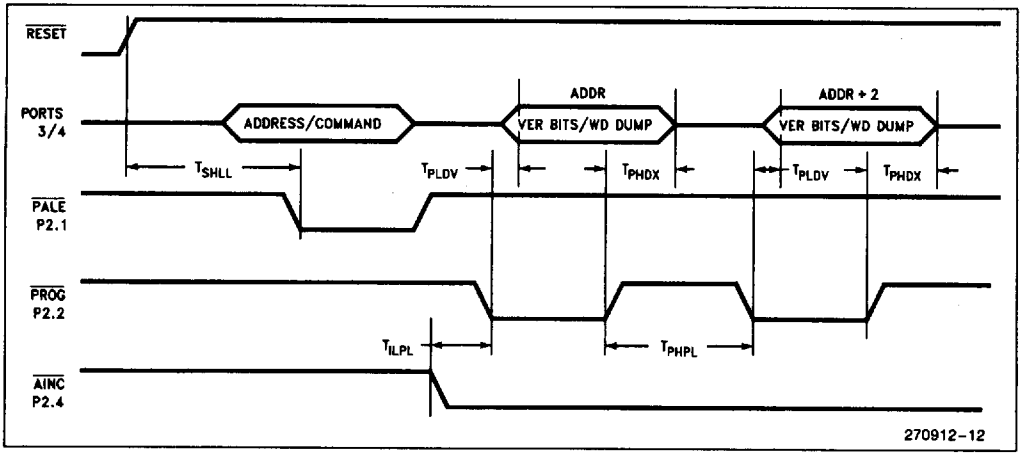
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

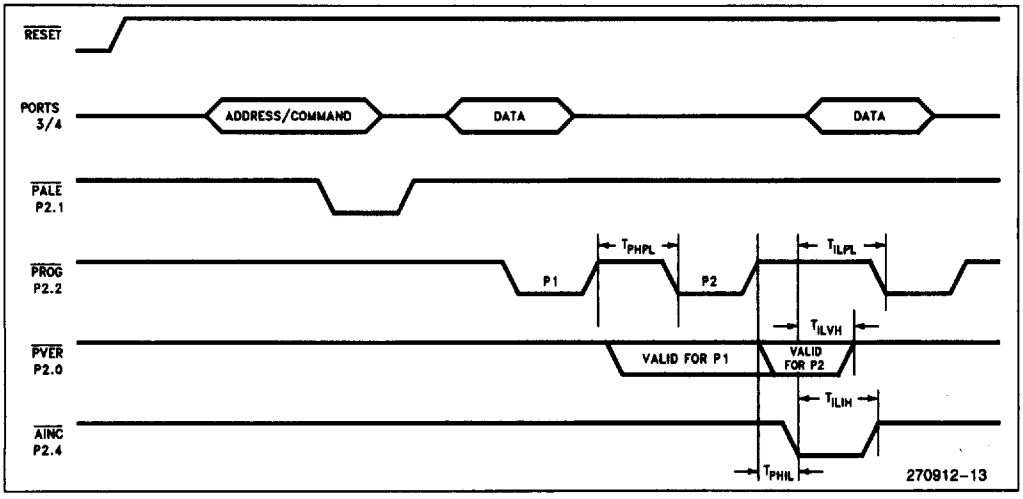
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196KR/87C196JR ERRATA

1. I_{OH2}

Current devices do not meet the test condition for V_{OH2} of -15 µA. Instead the devices are guaranteed to source a minimum of -6 µA.

87C196KR/87C196JR DESIGN CONSIDERATIONS

1. EPA Timers

Special care must be taken when resetting/writing the EPA timers. This is more of a software technique than a device errata. For example: The EPA timers do not generate a "time valid" signal when the counter is either reset or written. This means that if a compare event is programmed in the EPA/Compare channel for a value of "0000H" (when reset) or equal to a written value, the compared event will NOT happen. However, if the timers are allowed to increment/decrement to that value, that compare event WILL occur.

2. Port 6.4, 6.5, 6.6, 6.7

The user is not allowed to modify the P6_REG register when these pins are configured as Special Function P6_MODE.x = 1). During software manipulation of these registers, it is a good practice to first change the P6_MODE register, then modify the P6_REG register when switching from SF to LSIO.

3. P2.7 (CLKOUT)

Port 2.7 (CLKOUT) does not operate in open drain mode.

4. Current versions of the 8XC196KQ/JQ are fabricated with 16K of internal OTPROM, 512 bytes of register RAM, and 256 bytes of internal RAM. The memory map of the 8XC196KQ/JQ is identical to the 8XC196KR/JR. However, the extra memory locations are not tested and should not be used. Intel may disable this extra memory on future versions of the 8XC196KQ/JQ. Any software that relies on reading or writing these locations may not function correctly on future devices.

   Two steps the user should always incorporate to insure future compatibility are:

   A) The program must contain a jump to a location greater than 16K before the 12K boundary is reached. This is necessary only if greater than 12K of program memory is required and portions of the program executes from internal OTPROM.

   B) Use program memory from 12K to 16K only if $\overline{EA}$ is tied to ground. Never use data memory from 180H to 1FFH or from 480H to 4FFH.

4

52-LEAD DEVICES

Intel offers a 52-lead version of the 87C196KR device: the 87C196JR and 87C196JQ devices.

It is important to point out some functionality differences because of future devices or to remain software consistent with the 68-lead device. Because of the absence of pins on the 52-lead device some functions are not supported.

52-Lead Unsupported Functions:
- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer1
- WRH or BHE Functions
- Dynamic Buswidth
- Dynamic Wait State Control

The following is a list of recommended practices when using the 52-lead device:

(1) **External Memory.** Use an 8-bit bus mode only. There is neither a WRH or BUSWIDTH pin. The bus cannot dynamically switch from 8- to 16-bit or vice versa. Set the CCB bytes to an 8-bit only mode, using WR function only.

(2) **Wait State Control.** Use the CCB bytes to configure the maximum number of wait states. If the READY pin is selected to be a system function, the device will lockup waiting for READY. If the READY pin is configured as LSIO (default after RESET), the internal logic will receive a logic "0" level and insert the CCB defined number of wait states in the bus cycle. DON'T USE IRC = "111".

(3) **NMI Support.** The NMI is not bonded out. Make the NMI vector at location 203Eh vector to a Return instruction. This is for glitch safety protection only.

(4) **Auto-Programming Mode.** The 52-lead device will ONLY support the 16-bit zero wait state bus during auto-programming.

(5) **EPA4 through EPA7.** Since the JR and JQ devices use the KR silicon, these functions are in the device, just not bonded out. A programmer can use these as compare only channels or for other functions like software timer, start and A/D, or reset timers.

(6) **Slave Port Support.** The Slave port can still be used on the 52-lead devices. The only function removed is the SLPINT output function.

(7) **Port Functions.** Some port pins have been removed. P5.7, P5.6, P5.5, P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The Px_REG, Px_MODE, and Px_DIR registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

Additionally, these port pins should be setup internally by software as follows:

1. Written to Px_REG as "1" or "0".
2. Configured as Push/Pull, Px_DIR as "0".
3. Configured as LSIO.

This configuration will effectively strap the pin either high or low. *DO NOT Configure as Open Drain output "1", or as an Input pin. This device is CMOS.*

REVISION HISTORY

This data sheet (270912-003) supercedes 270912-002 and is valid for devices with a "C" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify that you have the latest version before finalizing a design or ordering devices.

1. Removed the following errata:
   - Slave Programming Mode
   - EPA__MASK1/EPA__PEND1
   - BMOVI
   - PTS and Other Interrupts
   - Serial Port Framing Error
   - Remap Mode on EPA3
   - A/D Abort
   - PTS/NMI Conflict
   - Data Output Register Cleared
   - Divide Error during HOLD/READY
   - SIO Mode 0
   - EPAIPV Multiplied by Two
   - (These were fixed on the C-step)
2. Moved the following from Errata to Design Considerations:
   - EPA Timers
   - Port 6.4, 6.5, 6.6, 6.7 (and reworded)
   - P2.7 (CLKOUT)
   - Oscillator Noise Sensitivity
3. Added New Errata:
   - I_{OH2} (also existed on A-step)
4. Added SLPCS to Package Diagrams and Pin Descriptions
5. Added T_{BVLL}
6. Added I_{IH} for NMI
7. Added notes to AC Characteristics identifying specifications that do not apply to JR/JQ
8. Changed T_{CLLH} from −5 ns to −10 ns under HOLD/HLDA Timings
9. Changed T_{HVCH} from 55 ns to 65 ns
10. Changed T_{AZHAL} from 10 ns to 25 ns
11. Changed T_{BZHAL} from 10 ns to 25 ns
12. Changed I_{CC} (max) from 70 mA to 75 mA
13. Changed I_{CC} formula from (3.88 × Freq + 8.43) to (3.88X Freq + 13.43)
14. Changed V_{OH2} test point from −50 μA to −15 μA
15. Changed Note 1 in DC parameters
16. Changed External Clock min/max, high/low times from percentage to ratio of T_{OSC}
17. Removed NMI from standard inputs (Note 2 under DC Characteristics)
18. Removed V_{OL1} spec
19. Removed T_{CLBV}
20. Added JQ/KQ design consideration

Data sheet 270912-002 supercedes 270912-001 and is valid for devices with an "A" at the end of the topside tracking number.

1. Removed:
   - CPU features descriptions
   - Peripheral features descriptions
   - SFR Operation (placed in Quick Reference)
   - SFR Maps (placed in Quick Reference)
   - SFR Bit Maps (placed in Quick Reference)
   - I_{IL} in DC Characteristics
   - T_{CLHAL} Max and T_{CLBRH} Max
   - Incorrect Sample and Convert time table from 8-bit A/D
2. Added:
   - Express options
   - Bullets on front page
   - Memory Map
   - Process Information
   - Prefix Identification
   - Thermal Characteristics
   - Programming functions to pin-out and pin descriptions
   - Ambient Temperature under Bias to Absolute Maximum Ratings
   - Note relating to Power Dissipation in Absolute Maximum Rating
   - Notes 8 and 9 to DC Characteristics
   - T_{CLBV} to AC Characteristics
   - Title to Buswidth timing diagram
   - T_{YLYH} to Buswidth timing diagram
   - Hold latency spec
   - External Crystal Connection diagram
   - External Clock Connection diagram
   - 10-bit A/D Operating Conditions Table
   - Title to 10-bit and 8-bit mode A/D Characteristics
   - Voltage on Analog Input Pin specification
   - Sampling Capacitor typical value
   - Note 4 to 10-bit and 8-bit A/D Specifications
   - 8-bit A/D Operating Conditions Table

Off Isolation, Feedthrough, V_{CC} Power Supply Rejection, Input Series Resistance, Voltage on Analog Input Pin, Sampling Capacitor and DC Input Leakage to 8-bit A/D specifications

Notes 1, 2 and 3 to EPROM Programming Conditions

New Errata (Items 10 to 16)

3. Changed:

Title of data sheet from "8XC196KR/KQ/JR/JQ 16-BIT HIGH PERFORMANCE CHMOS MICROCONTROLLER" to "8XC196KR/KQ/JR/JQ COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER"

Several bullets on cover sheet

Register RAM numbers in table on front page to match device

Operating conditions to tabular format

Note 1 in DC Characteristics to include Ports 3 and 4

0 to V_{SS} for I_{LI} and I_{LI1} in DC Characteristics

Format of symbols in AC Characteristics

T_{CLCH} to T_{CLLH} in System Bus Timing diagram

T_{XLXL} Max from 286 ns to 250 ns

T_{XHXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXH} from T_{OSC} − 50 ns to 10 ns

T_{XHXL} from T_{OSC} − 50 ns to 10 ns

AC Testing Input, Output Waveform

Introductory text on A to D Characteristics and Converter Specification

DC Input Leakage from ±1 μA to ±3 μA in A/D Specifications.

Power Dissipation from 0.5W to 1.0W.

Wording in Float Waveform from 100 mV to 150 mV.

EPROM Programming Characteristics to Operating Conditions table.

Data sheet (270912-001) is valid for devices with an "A" at the end of the topside tracking number. This is the first version of the data sheet.