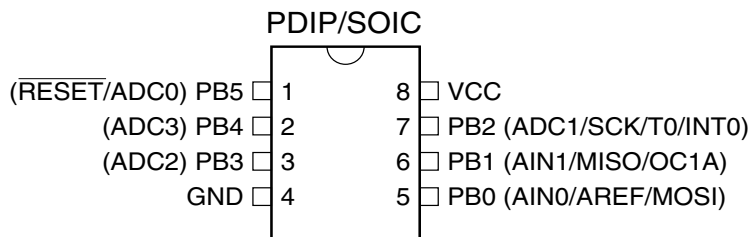


## Features

- High-performance, Low-power AVR<sup>®</sup> 8-bit Microcontroller
- Advanced RISC Architecture
  - 90 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
- Nonvolatile Program and Data Memories
  - 1K Byte In-System Programmable Flash Program Memory  
Endurance: 1,000 Write/Erase Cycles
  - 64 Bytes EEPROM  
Endurance: 100,000 Write/Erase Cycles
  - Programming Lock for Flash Program Data Security
- Peripheral Features
  - Interrupt and Wake-up on Pin Change
  - Two 8-bit Timer/Counters with Separate Prescalers
  - One 150 kHz, 8-bit High-speed PWM Output
  - 4-channel 10-bit ADC  
One Differential Voltage Input with Optional Gain of 20x
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with On-chip Oscillator
- Special Microcontroller Features
  - In-System Programmable via SPI Port
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal, Calibrated 1.6 MHz Tunable Oscillator
  - Internal 25.6 MHz Clock Generator for Timer/Counter
  - External and Internal Interrupt Sources
  - Low-power Idle and Power-down Modes
- Power Consumption at 1.6 MHz, 3V, 25°C
  - Active: 3.0 mA
  - Idle Mode: 1.0 mA
  - Power-down: < 1  $\mu$ A
- I/O and Packages
  - 8-lead PDIP and 8-lead SOIC: 6 Programmable I/O Lines
- Operating Voltages
  - 2.7V - 5.5V
- Internal 1.6 MHz System Clock

## Pin Configuration



## 8-bit AVR<sup>®</sup> Microcontroller with 1K Byte Flash

ATtiny15L

Rev. 1187DS-12/01



Note: This is a summary document. A complete document is available on our web site at [www.atmel.com](http://www.atmel.com).

## Description

The ATtiny15L is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny15L achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

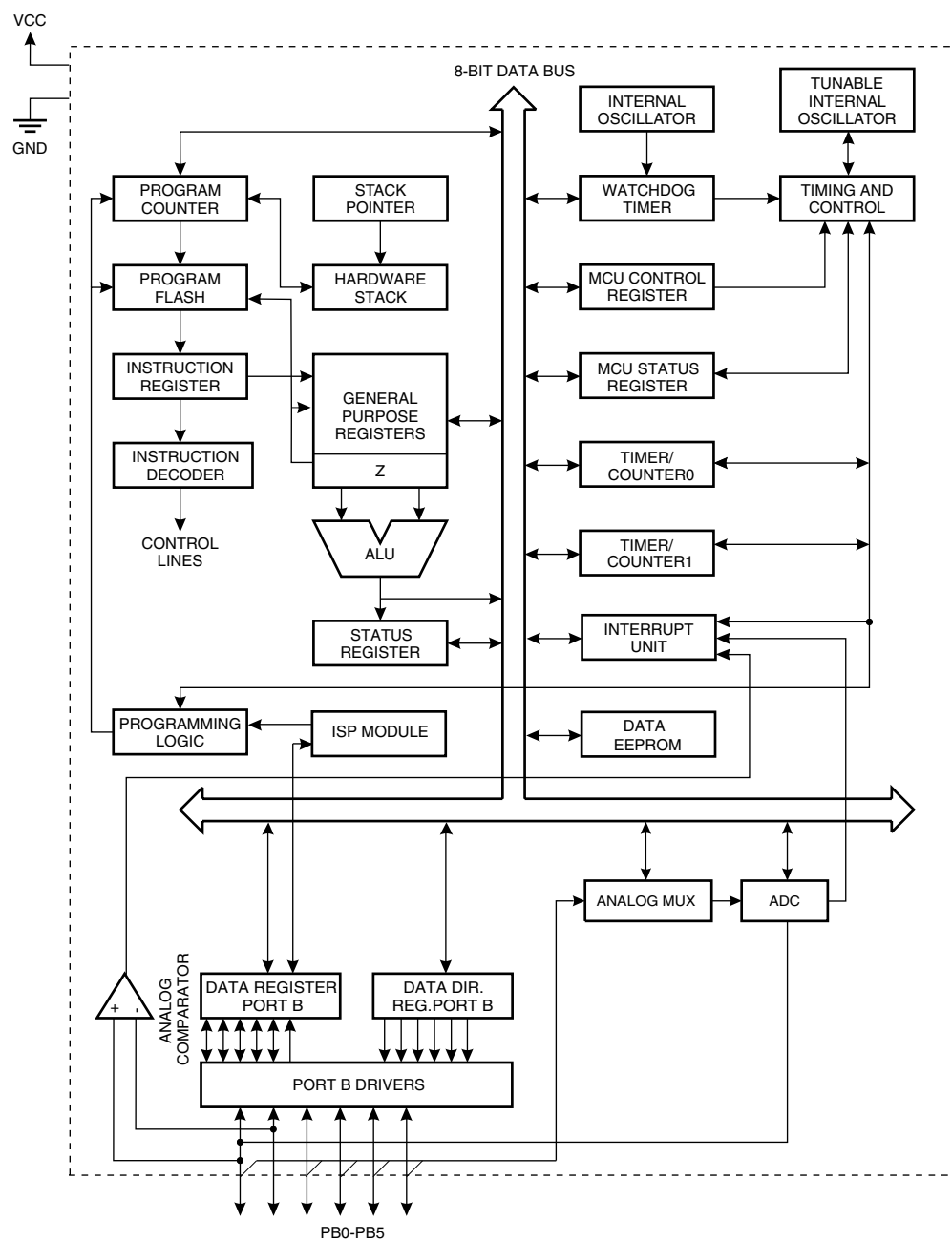
The ATtiny15L provides 1K byte of Flash, 64 bytes EEPROM, six general purpose I/O lines, 32 general purpose working registers, two 8-bit Timer/Counters, one with high-speed PWM output, internal oscillators, internal and external interrupts, programmable Watchdog Timer, 4-channel 10-bit Analog-to-Digital Converter with one differential voltage input with optional 20x gain, and three software-selectable Power-saving modes. The Idle mode stops the CPU while allowing the ADC, analog comparator, Timer/Counters and interrupt system to continue functioning. The ADC Noise Reduction mode facilitates high-accuracy ADC measurements by stopping the CPU while allowing the ADC to continue functioning. The Power-down mode saves the register contents but freezes the oscillators, disabling all other chip functions until the next interrupt or hardware reset. The wake-up or interrupt on pin change features enable the ATtiny15L to be highly responsive to external events, still featuring the lowest power consumption while in the Power-saving modes.

The device is manufactured using Atmel's high-density, nonvolatile memory technology. By combining a RISC 8-bit CPU with Flash on a monolithic chip, the ATtiny15L is a powerful microcontroller that provides a highly flexible and cost-efficient solution to many embedded control applications. The peripheral features make the ATtiny15L particularly suited for battery chargers, lighting ballasts and all kinds of intelligent sensor applications.

The ATtiny15L AVR is supported with a full suite of program and system development tools including macro assemblers, program debugger/simulators, In-circuit emulators and evaluation kits.

## Block Diagram

Figure 1. The ATtiny15L Block Diagram



## Pin Descriptions

|                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>VCC</b>               | Supply voltage pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>GND</b>               | Ground pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>Port B (PB5..PB0)</b> | <p>Port B is a 6-bit I/O port. PB4..0 are I/O pins that can provide internal pull-ups (selected for each bit). PB5 is input or open-drain output. The use of pin PB5 is defined by a fuse and the special function associated with this pin is external Reset. The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> <p>Port B also accommodates analog I/O pins. The Port B pins with alternate functions are shown in Table 1.</p> |

**Table 1.** Port B Alternate Functions

| Port Pin | Alternate Function                                                                                                                                              |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PB0      | MOSI (Data Input Line for Memory Downloading)<br>AREF (ADC Voltage Reference)<br>AIN0 (Analog Comparator Positive Input)                                        |
| PB1      | MISO (Data Output Line for Memory Downloading)<br>OC1A (Timer/Counter PWM Output)<br>AIN1 (Analog Comparator Negative Input)                                    |
| PB2      | SCK (Serial Clock Input for Serial Programming)<br>INT0 (External Interrupt0 Input)<br>ADC1 (ADC Input Channel 1)<br>T0 (Timer/Counter0 External Counter Input) |
| PB3      | ADC2 (ADC Input Channel 2)                                                                                                                                      |
| PB4      | ADC3 (ADC Input Channel 3)                                                                                                                                      |
| PB5      | $\overline{\text{RESET}}$ (External Reset Pin)<br>ADC0 (ADC Input Channel 0)                                                                                    |

**Analog Pins** Up to four analog inputs can be selected as inputs to Analog-to-Digital Converter (ADC).

## Internal Oscillators

The internal oscillator provides a clock rate of nominally 1.6 MHz for the system clock (CK). Due to large initial variation (0.8 -1.6 MHz) of the internal oscillator, a tuning capability is built in. Through an 8-bit control register – OSCCAL – the system clock rate can be tuned with less than 1% steps of the nominal clock.

There is an internal PLL that provides a 16x clock rate locked to the system clock (CK) for the use of the Peripheral Timer/Counter1. The nominal frequency of this peripheral clock, PCK, is 25.6 MHz.

## ATtiny15L Register Summary

| Address | Name     | Bit 7                                            | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Page    |
|---------|----------|--------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|---------|
| \$3F    | SREG     | I                                                | T      | H      | S      | V      | N      | Z      | C      | page 11 |
| \$3E    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$3C    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$3B    | GIMSK    | -                                                | INT0   | PCIE   | -      | -      | -      | -      | -      | page 19 |
| \$3A    | GIFR     | -                                                | INTF0  | PCIF   | -      | -      | -      | -      | -      | page 19 |
| \$39    | TIMSK    | -                                                | OCIE1A | -      | -      | -      | TOIE1  | TOIE0  | -      | page 20 |
| \$38    | TIFR     | -                                                | OCF1A  | -      | -      | -      | TOV1   | TOV0   | -      | page 21 |
| \$37    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$36    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$35    | MCUCR    | -                                                | PUD    | SE     | SM1    | SM0    | -      | ISC01  | ISC00  | page 22 |
| \$34    | MCUSR    | -                                                | -      | -      | -      | WDRF   | BORF   | EXTRF  | PORF   | page 17 |
| \$33    | TCCR0    | -                                                | -      | -      | -      | -      | CS02   | CS01   | CS00   | page 27 |
| \$32    | TCNT0    | Timer/Counter0 (8-Bit)                           |        |        |        |        |        |        |        | page 28 |
| \$31    | OSCCAL   | Oscillator Calibration Register                  |        |        |        |        |        |        |        | page 24 |
| \$30    | TCCR1    | CTC1                                             | PWM1   | COM1A1 | COM1A0 | CS13   | CS12   | CS11   | CS10   | page 30 |
| \$2F    | TCNT1    | Timer/Counter1 (8-Bit)                           |        |        |        |        |        |        |        | page 31 |
| \$2E    | OCR1A    | Timer/Counter1 Output Compare Register A (8-Bit) |        |        |        |        |        |        |        | page 31 |
| \$2D    | OCR1B    | Timer/Counter1 Output Compare Register B (8-Bit) |        |        |        |        |        |        |        | page 33 |
| \$2C    | SFIOR    | -                                                | -      | -      | -      | -      | FOC1A  | PSR1   | PSR0   | page 26 |
| \$2B    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$2A    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$29    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$28    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$27    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$26    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$25    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$24    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$23    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$22    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$21    | WDTCR    | -                                                | -      | -      | WDTOE  | WDE    | WDP2   | WDP1   | WDP0   | page 34 |
| \$20    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$1F    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$1E    | EEAR     | -                                                | -      | EEAR5  | EEAR4  | EEAR3  | EEAR2  | EEAR1  | EEAR0  | page 36 |
| \$1D    | EEDR     | EEPROM Data Register (8-Bit)                     |        |        |        |        |        |        |        | page 36 |
| \$1C    | EECR     | -                                                | -      | -      | -      | EERIE  | EEMWE  | EEWE   | EERE   | page 36 |
| \$1B    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$1A    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$19    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$18    | PORTB    | -                                                | -      | -      | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 51 |
| \$17    | DDRB     | -                                                | -      | DDB5   | DDB4   | DDB3   | DDB2   | DDB1   | DDB0   | page 51 |
| \$16    | PINB     | -                                                | -      | PINB5  | PINB4  | PINB3  | PINB2  | PINB1  | PINB0  | page 51 |
| \$15    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$14    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$13    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$12    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$11    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$10    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0F    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0E    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0D    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0C    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0B    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$0A    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$09    | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$08    | ACSR     | ACD                                              | ACBG   | ACO    | ACI    | ACIE   | -      | ACIS1  | ACIS0  | page 39 |
| \$07    | ADMUX    | REFS1                                            | REFS0  | ADLAR  | -      | -      | MUX2   | MUX1   | MUX0   | page 46 |
| \$06    | ADCSR    | ADEN                                             | ADSC   | ADFR   | ADIF   | ADIE   | ADPS2  | ADPS1  | ADPS0  | page 47 |
| \$05    | ADCH     | ADC Data Register High Byte                      |        |        |        |        |        |        |        | page 48 |
| \$04    | ADCL     | ADC Data Register Low Byte                       |        |        |        |        |        |        |        | page 48 |
| ...     | Reserved |                                                  |        |        |        |        |        |        |        |         |
| \$00    | Reserved |                                                  |        |        |        |        |        |        |        |         |



## ATTiny15L Instruction Set Summary

| Mnemonic                                 | Operands | Description                            | Operation                                             | Flags     | # Clocks |
|------------------------------------------|----------|----------------------------------------|-------------------------------------------------------|-----------|----------|
| <b>ARITHMETIC AND LOGIC INSTRUCTIONS</b> |          |                                        |                                                       |           |          |
| ADD                                      | Rd, Rr   | Add Two Registers                      | $Rd \leftarrow Rd + Rr$                               | Z,C,N,V,H | 1        |
| ADC                                      | Rd, Rr   | Add with Carry Two Registers           | $Rd \leftarrow Rd + Rr + C$                           | Z,C,N,V,H | 1        |
| SUB                                      | Rd, Rr   | Subtract Two Registers                 | $Rd \leftarrow Rd - Rr$                               | Z,C,N,V,H | 1        |
| SUBI                                     | Rd, K    | Subtract Constant from Register        | $Rd \leftarrow Rd - K$                                | Z,C,N,V,H | 1        |
| SBC                                      | Rd, Rr   | Subtract with Carry Two Registers      | $Rd \leftarrow Rd - Rr - C$                           | Z,C,N,V,H | 1        |
| SBCI                                     | Rd, K    | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$                            | Z,C,N,V,H | 1        |
| AND                                      | Rd, Rr   | Logical AND Registers                  | $Rd \leftarrow Rd \cdot Rr$                           | Z,N,V     | 1        |
| ANDI                                     | Rd, K    | Logical AND Register and Constant      | $Rd \leftarrow Rd \cdot K$                            | Z,N,V     | 1        |
| OR                                       | Rd, Rr   | Logical OR Registers                   | $Rd \leftarrow Rd \vee Rr$                            | Z,N,V     | 1        |
| ORI                                      | Rd, K    | Logical OR Register and Constant       | $Rd \leftarrow Rd \vee K$                             | Z,N,V     | 1        |
| EOR                                      | Rd, Rr   | Exclusive OR Registers                 | $Rd \leftarrow Rd \oplus Rr$                          | Z,N,V     | 1        |
| COM                                      | Rd       | One's Complement                       | $Rd \leftarrow \$FF - Rd$                             | Z,C,N,V   | 1        |
| NEG                                      | Rd       | Two's Complement                       | $Rd \leftarrow \$00 - Rd$                             | Z,C,N,V,H | 1        |
| SBR                                      | Rd, K    | Set Bit(s) in Register                 | $Rd \leftarrow Rd \vee K$                             | Z,N,V     | 1        |
| CBR                                      | Rd, K    | Clear Bit(s) in Register               | $Rd \leftarrow Rd \cdot (\text{FFh} - K)$             | Z,N,V     | 1        |
| INC                                      | Rd       | Increment                              | $Rd \leftarrow Rd + 1$                                | Z,N,V     | 1        |
| DEC                                      | Rd       | Decrement                              | $Rd \leftarrow Rd - 1$                                | Z,N,V     | 1        |
| TST                                      | Rd       | Test for Zero or Minus                 | $Rd \leftarrow Rd \cdot Rd$                           | Z,N,V     | 1        |
| CLR                                      | Rd       | Clear Register                         | $Rd \leftarrow Rd \oplus Rd$                          | Z,N,V     | 1        |
| SER                                      | Rd       | Set Register                           | $Rd \leftarrow \$FF$                                  | None      | 1        |
| <b>BRANCH INSTRUCTIONS</b>               |          |                                        |                                                       |           |          |
| RJMP                                     | k        | Relative Jump                          | $PC \leftarrow PC + k + 1$                            | None      | 2        |
| RCALL                                    | k        | Relative Subroutine Call               | $PC \leftarrow PC + k + 1$                            | None      | 3        |
| RET                                      |          | Subroutine Return                      | $PC \leftarrow \text{STACK}$                          | None      | 4        |
| RETI                                     |          | Interrupt Return                       | $PC \leftarrow \text{STACK}$                          | I         | 4        |
| CPSE                                     | Rd, Rr   | Compare, Skip if Equal                 | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3            | None      | 1/2      |
| CP                                       | Rd, Rr   | Compare                                | $Rd - Rr$                                             | Z,N,V,C,H | 1        |
| CPC                                      | Rd, Rr   | Compare with Carry                     | $Rd - Rr - C$                                         | Z,N,V,C,H | 1        |
| CPI                                      | Rd, K    | Compare Register with Immediate        | $Rd - K$                                              | Z,N,V,C,H | 1        |
| SBRC                                     | Rr, b    | Skip if Bit in Register Cleared        | if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3          | None      | 1/2      |
| SBRS                                     | Rr, b    | Skip if Bit in Register is Set         | if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3          | None      | 1/2      |
| SBIC                                     | P, b     | Skip if Bit in I/O Register Cleared    | if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3           | None      | 1/2      |
| SBIS                                     | P, b     | Skip if Bit in I/O Register is Set     | if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3           | None      | 1/2      |
| BRBS                                     | s, k     | Branch if Status Flag Set              | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$    | None      | 1/2      |
| BRBC                                     | s, k     | Branch if Status Flag Cleared          | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$    | None      | 1/2      |
| BREQ                                     | k        | Branch if Equal                        | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRNE                                     | k        | Branch if Not Equal                    | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRCS                                     | k        | Branch if Carry Set                    | if $(C = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRCC                                     | k        | Branch if Carry Cleared                | if $(C = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRSH                                     | k        | Branch if Same or Higher               | if $(C = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRLO                                     | k        | Branch if Lower                        | if $(C = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRMI                                     | k        | Branch if Minus                        | if $(N = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRPL                                     | k        | Branch if Plus                         | if $(N = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRGE                                     | k        | Branch if Greater or Equal, Signed     | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$ | None      | 1/2      |
| BRLT                                     | k        | Branch if Less Than Zero, Signed       | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$ | None      | 1/2      |
| BRHS                                     | k        | Branch if Half-carry Flag Set          | if $(H = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRHC                                     | k        | Branch if Half-carry Flag Cleared      | if $(H = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRTS                                     | k        | Branch if T-flag Set                   | if $(T = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRTC                                     | k        | Branch if T-flag Cleared               | if $(T = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRVS                                     | k        | Branch if Overflow Flag is Set         | if $(V = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRVC                                     | k        | Branch if Overflow Flag is Cleared     | if $(V = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRIE                                     | k        | Branch if Interrupt Enabled            | if $(I = 1)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| BRID                                     | k        | Branch if Interrupt Disabled           | if $(I = 0)$ then $PC \leftarrow PC + k + 1$          | None      | 1/2      |
| <b>DATA TRANSFER INSTRUCTIONS</b>        |          |                                        |                                                       |           |          |
| LD                                       | Rd, Z    | Load Register Indirect                 | $Rd \leftarrow (Z)$                                   | None      | 2        |
| ST                                       | Z, Rr    | Store Register Indirect                | $(Z) \leftarrow Rr$                                   | None      | 2        |
| MOV                                      | Rd, Rr   | Move between Registers                 | $Rd \leftarrow Rr$                                    | None      | 1        |
| LDI                                      | Rd, K    | Load Immediate                         | $Rd \leftarrow K$                                     | None      | 1        |
| IN                                       | Rd, P    | In Port                                | $Rd \leftarrow P$                                     | None      | 1        |
| OUT                                      | P, Rr    | Out Port                               | $P \leftarrow Rr$                                     | None      | 1        |
| LPM                                      |          | Load Program Memory                    | $R0 \leftarrow (Z)$                                   | None      | 3        |
| <b>BIT AND BIT-TEST INSTRUCTIONS</b>     |          |                                        |                                                       |           |          |
| SBI                                      | P, b     | Set Bit in I/O Register                | $I/O(P,b) \leftarrow 1$                               | None      | 2        |

**ATtiny15L Instruction Set Summary (Continued)**

| Mnemonic | Operands | Description                     | Operation                                                          | Flags   | # Clocks |
|----------|----------|---------------------------------|--------------------------------------------------------------------|---------|----------|
| CBI      | P, b     | Clear Bit in I/O Register       | $I/O(P,b) \leftarrow 0$                                            | None    | 2        |
| LSL      | Rd       | Logical Shift Left              | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$                     | Z,C,N,V | 1        |
| LSR      | Rd       | Logical Shift Right             | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$                     | Z,C,N,V | 1        |
| ROL      | Rd       | Rotate Left through Carry       | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1        |
| ROR      | Rd       | Rotate Right through Carry      | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1        |
| ASR      | Rd       | Arithmetic Shift Right          | $Rd(n) \leftarrow Rd(n+1), n = 0..6$                               | Z,C,N,V | 1        |
| SWAP     | Rd       | Swap Nibbles                    | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$       | None    | 1        |
| BSET     | s        | Flag Set                        | $SREG(s) \leftarrow 1$                                             | SREG(s) | 1        |
| BCLR     | s        | Flag Clear                      | $SREG(s) \leftarrow 0$                                             | SREG(s) | 1        |
| BST      | Rr, b    | Bit Store from Register to T    | $T \leftarrow Rr(b)$                                               | T       | 1        |
| BLD      | Rd, b    | Bit Load from T to Register     | $Rd(b) \leftarrow T$                                               | None    | 1        |
| SEC      |          | Set Carry                       | $C \leftarrow 1$                                                   | C       | 1        |
| CLC      |          | Clear Carry                     | $C \leftarrow 0$                                                   | C       | 1        |
| SEN      |          | Set Negative Flag               | $N \leftarrow 1$                                                   | N       | 1        |
| CLN      |          | Clear Negative Flag             | $N \leftarrow 0$                                                   | N       | 1        |
| SEZ      |          | Set Zero Flag                   | $Z \leftarrow 1$                                                   | Z       | 1        |
| CLZ      |          | Clear Zero Flag                 | $Z \leftarrow 0$                                                   | Z       | 1        |
| SEI      |          | Global Interrupt Enable         | $I \leftarrow 1$                                                   | I       | 1        |
| CLI      |          | Global Interrupt Disable        | $I \leftarrow 0$                                                   | I       | 1        |
| SES      |          | Set Signed Test Flag            | $S \leftarrow 1$                                                   | S       | 1        |
| CLS      |          | Clear Signed Test Flag          | $S \leftarrow 0$                                                   | S       | 1        |
| SEV      |          | Set Two's Complement Overflow   | $V \leftarrow 1$                                                   | V       | 1        |
| CLV      |          | Clear Two's Complement Overflow | $V \leftarrow 0$                                                   | V       | 1        |
| SET      |          | Set T in SREG                   | $T \leftarrow 1$                                                   | T       | 1        |
| CLT      |          | Clear T in SREG                 | $T \leftarrow 0$                                                   | T       | 1        |
| SEH      |          | Set Half-carry Flag in SREG     | $H \leftarrow 1$                                                   | H       | 1        |
| CLH      |          | Clear Half-carry Flag in SREG   | $H \leftarrow 0$                                                   | H       | 1        |
| NOP      |          | No Operation                    |                                                                    | None    | 1        |
| SLEEP    |          | Sleep                           | (see specific descr. for Sleep function)                           | None    | 1        |
| WDR      |          | Watchdog Reset                  | (see specific descr. for WDR/timer)                                | None    | 1        |



## Ordering Information

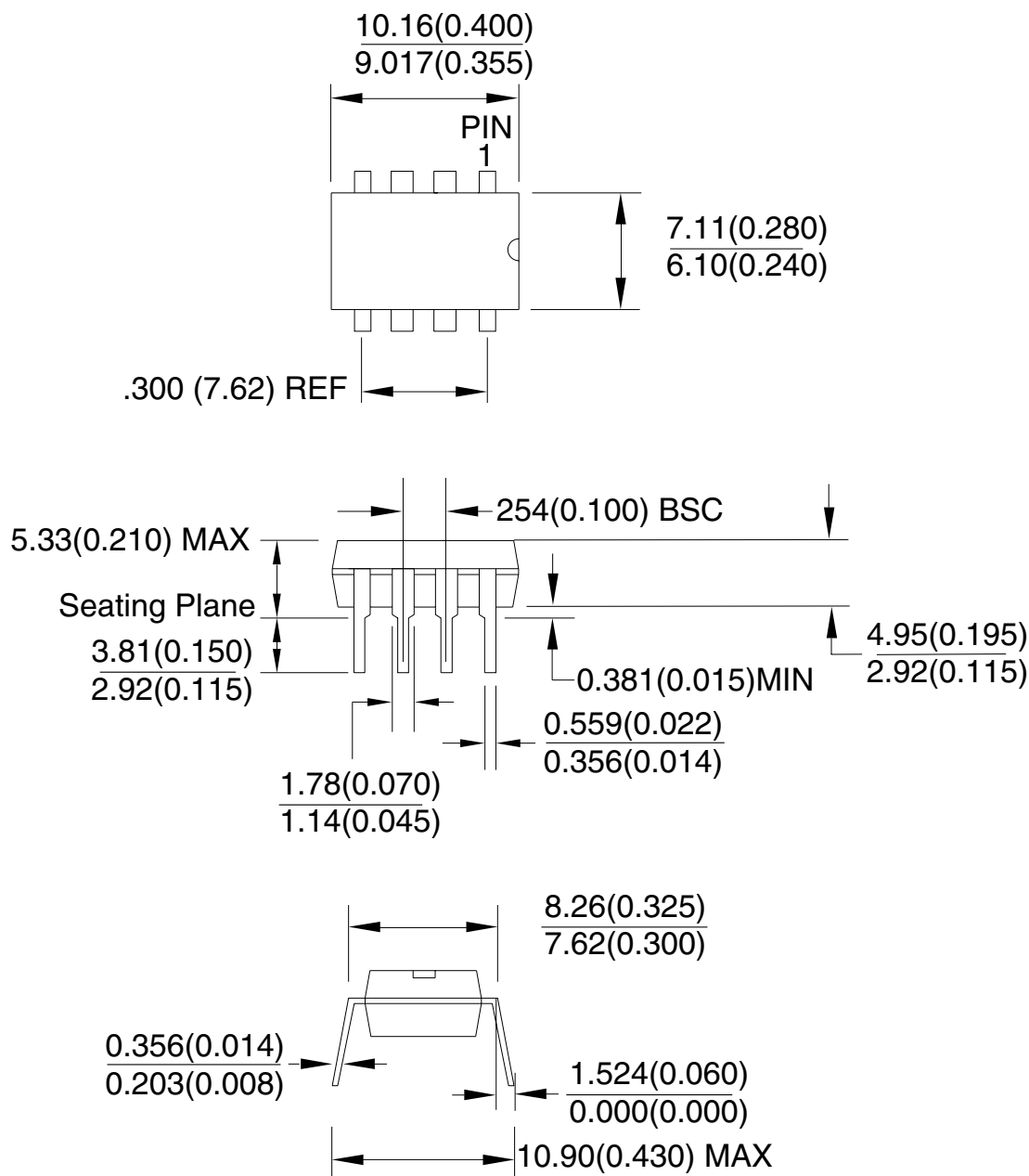
| Power Supply | Speed (MHz) | Ordering Code | Package | Operation Range               |
|--------------|-------------|---------------|---------|-------------------------------|
| 2.7 - 5.5V   | 1.6         | ATtiny15L-1PC | 8P3     | Commercial<br>(0°C to 70°C)   |
|              |             | ATtiny15L-1SC | 8S2     |                               |
|              |             | ATtiny15L-1PI | 8P3     | Industrial<br>(-40°C to 85°C) |
|              |             | ATtiny15L-1SI | 8S2     |                               |

| Package Type |                                                                  |
|--------------|------------------------------------------------------------------|
| 8P3          | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)          |
| 8S2          | 8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC) |

## Packaging Information

### 8P3

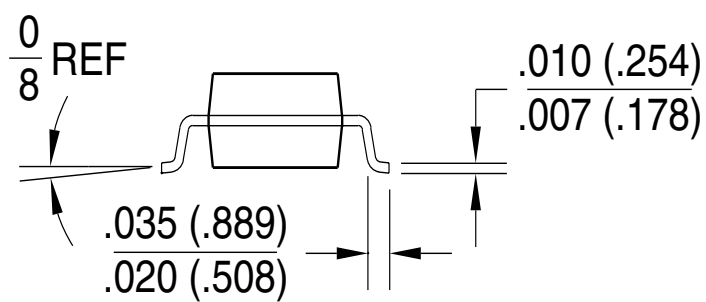
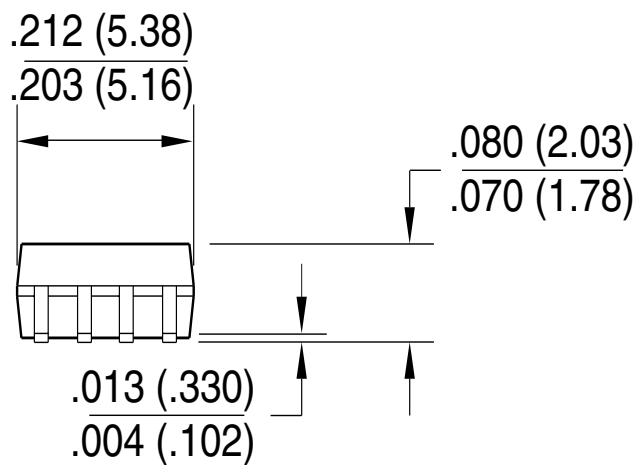
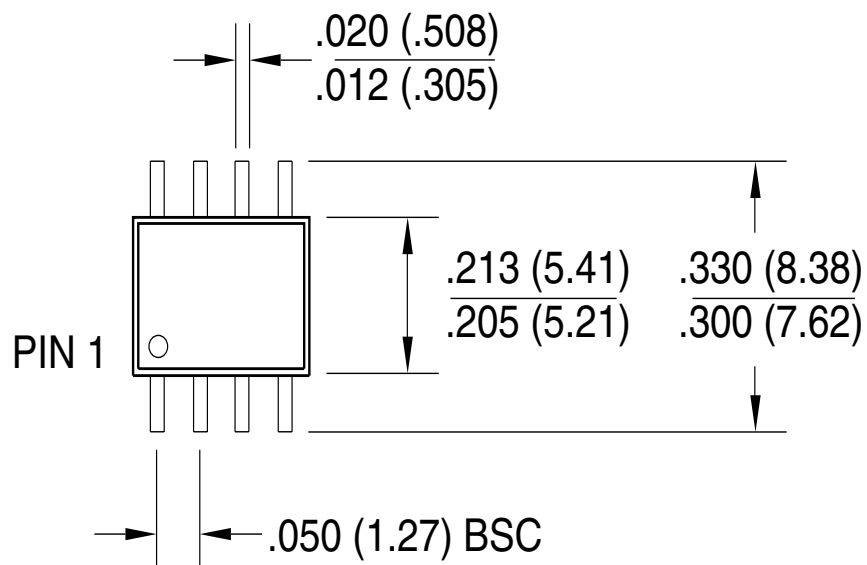
8P3, 8-lead, Plastic Dual Inline  
 Package (PDIP), 0.300" Wide.  
 Dimensions in Millimeters and (Inches)\*  
 JEDEC STANDARD MS-001 BA



\*Controlling dimension: Inches

REV. A 04/11/2001

8S2





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