

PRELIMINARY

- **High Speed (Equal Access and Cycle Times)**
  - 20/25/30/35 ns (Commercial)
  - 25/30/35/45/55 ns (Military)
- **Low Power (Commercial/Military)**
  - 690 mW Active – 20
  - 605/660 mW Active – 25/30/35/45/55
  - 135/220 mW Standby (TTL Input)
  - 55/110 mW Standby (CMOS Input) P4C1281/82
  - 9/12 mW Standby (CMOS Input) P4C1281L/82L
- **5V  $\pm$  10% Power Supply**

- **Data Retention with 2.0V Supply**
- **Separate Inputs and Outputs**
  - P4C1281/L Input Data at Outputs during Write
  - P4C1282/L Outputs in High Z during Write
- **Fully TTL Compatible Inputs and Outputs**
- **Produced with PACE II Technology™**
- **Standard Pinout (JEDEC Approved)**
  - 28-Pin 300 mil DIP, SOJ
  - 28-Pin 350 x 550 mil LCC

The P4C1282/L and P4C1281/L are 262,144-bit (64K x 4) ultra high speed static RAMs similar to the P4C1298, but with separate data I/O pins. The P4C1281/L feature a transparent write operation when  $\overline{OE}$  is low; the outputs of the P4C1282/L are in high impedance during the write cycle. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V  $\pm 10\%$  tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10  $\mu$ A from 2.0V supply.

Access times as fast as 20 nanoseconds are available, permitting greatly enhanced system operating speeds.

CMOS is utilized to reduce power consumption to a low level in both active and standby modes. The P4C1282/L and P4C1281/L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C1282/L and P4C1281/L are manufactured with PACE II Technology™.

The P4C1282/L and P4C1281/L are available in 28-pin 300 mil DIP and SOJ, and in 28-pin 350x550 mil LCC packages providing excellent board level densities.

[illegible]

**DIP (P5, C5), SQJ (J5)**  
**TOP VIEW**

**LCC (L5)**  
**TOP VIEW**

1549 02



**Means Quality, Service and Speed**

©1989 Performance Semiconductor Corporation



## MAXIMUM RATINGS<sup>(1)</sup>

| Symbol     | Parameter                                         | Value                  | Unit |
|------------|---------------------------------------------------|------------------------|------|
| $V_{CC}$   | Power Supply Pin with Respect to GND              | -0.5 to +7             | V    |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to $V_{CC} + 0.5$ | V    |
| $T_A$      | Operating Temperature                             | -55 to +125            | °C   |

1549 Tbl 01

| Symbol     | Parameter              | Value       | Unit |
|------------|------------------------|-------------|------|
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C   |
| $T_{STG}$  | Storage Temperature    | -65 to +150 | °C   |
| $P_T$      | Power Dissipation      | 1.0         | W    |
| $I_{OUT}$  | DC Output Current      | 50          | mA   |

1549 Tbl 02

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Military             | -55 to +125°C       | 0V  | 5.0V ± 10% |

1549 Tbl 03

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Commercial           | 0°C to +70°C        | 0V  | 5.0V ± 10% |

1549 Tbl 04

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol           | Parameter                          | Test Conditions                                                                                           | P4C1281<br>P4C1282   |                      | P4C1281L<br>P4C1282L |                      | Unit |
|------------------|------------------------------------|-----------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------|----------------------|------|
|                  |                                    |                                                                                                           | Min                  | Max                  | Min                  | Max                  |      |
| V <sub>IH</sub>  | Input High Voltage                 |                                                                                                           | 2.2                  | V <sub>CC</sub> +0.5 | 2.2                  | V <sub>CC</sub> +0.5 | V    |
| V <sub>IL</sub>  | Input Low Voltage                  |                                                                                                           | -0.5 <sup>(3)</sup>  | 0.8                  | -0.5 <sup>(3)</sup>  | 0.8                  | V    |
| V <sub>HC</sub>  | CMOS Input High Voltage            |                                                                                                           | V <sub>CC</sub> -0.2 | V <sub>CC</sub> +0.5 | V <sub>CC</sub> -0.2 | V <sub>CC</sub> +0.5 | V    |
| V <sub>LC</sub>  | CMOS Input Low Voltage             |                                                                                                           | -0.5 <sup>(3)</sup>  | 0.2                  | -0.5 <sup>(3)</sup>  | 0.2                  | V    |
| V <sub>CD</sub>  | Input Clamp Diode Voltage          | V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA                                                          |                      | -1.2                 |                      | -1.2                 | V    |
| V <sub>OL</sub>  | Output Low Voltage<br>(TTL Load)   | I <sub>OL</sub> = +10 mA, V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = +8 mA, V <sub>CC</sub> = Min.       |                      | 0.5<br>0.4           |                      | 0.5<br>0.4           | V    |
| V <sub>OLC</sub> | Output Low Voltage<br>(CMOS Load)  | I <sub>OLC</sub> = +100 μA, V <sub>CC</sub> = Min.                                                        |                      | 0.2                  |                      | 0.2                  | V    |
| V <sub>OH</sub>  | Output High Voltage<br>(TTL Load)  | I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.                                                           | 2.4                  |                      | 2.4                  |                      | V    |
| V <sub>OHC</sub> | Output High Voltage<br>(CMOS Load) | I <sub>OHC</sub> = -100 μA, V <sub>CC</sub> = Min.                                                        | V <sub>CC</sub> -0.2 |                      | V <sub>CC</sub> -0.2 |                      | V    |
| I <sub>LI</sub>  | Input Leakage Current              | V <sub>CC</sub> = Max. Mil.<br>V <sub>IN</sub> = GND to V <sub>CC</sub> Com'l.                            | -10<br>-5            | +10<br>+5            | -5<br>-2             | +5<br>+2             | μA   |
| I <sub>LO</sub>  | Output Leakage Current             | V <sub>CC</sub> = Max., $\overline{CE} = V_{IH}$ Mil.<br>V <sub>OUT</sub> = GND to V <sub>CC</sub> Com'l. | -10<br>-5            | +10<br>+5            | -5<br>-2             | +5<br>+2             | μA   |

1549 Tbl 05

## CAPACITANCES<sup>(4)</sup>

 $(V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}, f = 1.0\text{MHz})$ 

| Symbol   | Parameter         | Conditions           | Typ. | Unit |
|----------|-------------------|----------------------|------|------|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0\text{V}$ | 5    | pF   |

1549 Tbl 06

| Symbol    | Parameter          | Conditions            | Typ. | Unit |
|-----------|--------------------|-----------------------|------|------|
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0\text{V}$ | 7    | pF   |

1549 Tbl 07

### Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with  $V_{IL}$  and  $I_{IL}$  not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol    | Parameter                                        | Test Conditions                                                                                                                                 | P4C1281<br>P4C1282 |            | P4C1281L<br>P4C1282L |            | Unit |
|-----------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------|----------------------|------------|------|
|           |                                                  |                                                                                                                                                 | Min                | Max        | Min                  | Max        |      |
| $I_{CC}$  | Dynamic Operating Current – 20                   | $V_{CC} = \text{Max.}, f = \text{Max.},$<br>Outputs Open Mil.<br>Com'l.                                                                         | —                  | n/a<br>125 | —                    | n/a<br>n/a | mA   |
| $I_{CC}$  | Dynamic Operating Current – 25, 30, 35, 45, 55   | $V_{CC} = \text{Max.}, f = \text{Max.},$<br>Outputs Open Mil.<br>Com'l.                                                                         | —                  | 120<br>110 | —                    | 120<br>110 | mA   |
| $I_{SB}$  | Standby Power Supply Current (TTL Input Levels)  | $\overline{CE} \geq V_{IH}$<br>$V_{CC} = \text{Max.},$<br>$f = \text{Max.},$ Outputs Open Mil.<br>Com'l.                                        | —                  | 35<br>35   | —                    | 35<br>35   | mA   |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE} \geq V_{HC}$<br>$V_{CC} = \text{Max.},$<br>$f = 0,$ Outputs Open,<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ Mil.<br>Com'l. | —                  | 35<br>30   | —                    | 1.0<br>0.2 | mA   |

n/a = Not Applicable

1549 Tbl 08

2

DATA RETENTION CHARACTERISTICS (P4C1281L and P4C1282L Only)

| Symbol        | Parameter                            | Test Condition                                                                              | Min         | Typ.*<br>$V_{CC} =$ |          | Max<br>$V_{CC} =$ |            | Unit                           |
|---------------|--------------------------------------|---------------------------------------------------------------------------------------------|-------------|---------------------|----------|-------------------|------------|--------------------------------|
|               |                                      |                                                                                             |             | 2.0V                | 3.0V     | 2.0V              | 3.0V       |                                |
| $V_{DR}$      | $V_{CC}$ for Data Retention          |                                                                                             | 2.0         |                     |          |                   |            | V                              |
| $I_{CCDR}$    | Data Retention Current               | Mil.<br>Com'l.                                                                              |             | 50<br>50            | 75<br>75 | 600<br>500        | 900<br>750 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $t_{CDR}$     | Chip Deselect to Data Retention Time | $\overline{CE} \geq V_{CC} - 0.2V,$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 0           |                     |          |                   |            | ns                             |
| $t_R^\dagger$ | Operation Recovery Time              |                                                                                             | $t_{RC}^\S$ |                     |          |                   |            | ns                             |

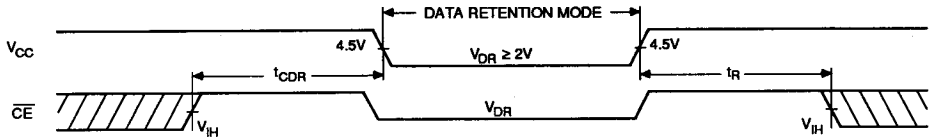
\* $T_A = +25^\circ\text{C}$

$t_{RC}^\S$  = Read Cycle Time

$^\dagger$  This parameter is guaranteed but not tested.

1549 Tbl 09

DATA RETENTION WAVEFORM



1549 03



## AC CHARACTERISTICS—READ CYCLE

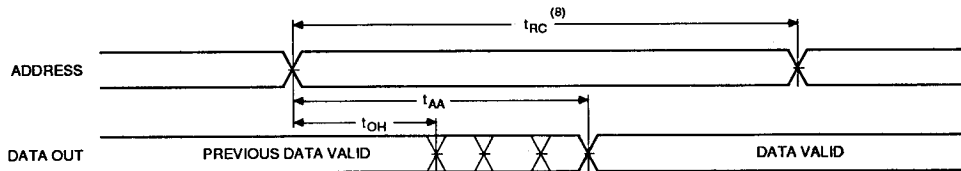
( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

| Symbol   | Parameter                        | -20* |     | -25 |     | -30 |     | -35 |     | -45 |     | -55 |     | Unit |
|----------|----------------------------------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|          |                                  | Min  | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| $t_{RC}$ | Read Cycle Time                  | 20   |     | 25  |     | 30  |     | 35  |     | 45  |     | 55  |     | ns   |
| $t_{AA}$ | Address Access Time              |      | 20  |     | 25  |     | 30  |     | 35  |     | 45  |     | 55  | ns   |
| $t_{AC}$ | Chip Enable Access Time          |      | 20  |     | 25  |     | 30  |     | 35  |     | 45  |     | 55  | ns   |
| $t_{OH}$ | Output Hold from Address Change  | 2    |     | 3   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| $t_{LZ}$ | Chip Enable to Output in Low Z   | 2    |     | 3   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| $t_{HZ}$ | Chip Disable to Output in High Z |      | 10  |     | 10  |     | 13  |     | 15  |     | 15  |     | 20  | ns   |
| $t_{PU}$ | Chip Enable to Power Up Time     | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{PD}$ | Chip Disable to Power Down Time  |      | 20  |     | 25  |     | 30  |     | 35  |     | 45  |     | 55  | ns   |

\* $V_{CC} = 5V \pm 5\%$  for -20

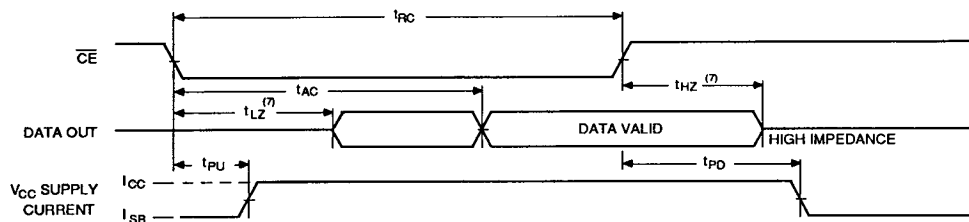
1549 Tbl 10

### TIMING WAVEFORM OF READ CYCLE NO. 1 <sup>(5)</sup>



1549 04

### TIMING WAVEFORM OF READ CYCLE NO. 2 <sup>(6)</sup>



1549 05

#### Notes:

5.  $\overline{CE}$  is low and  $\overline{WE}$  is high for READ cycle.
6.  $\overline{WE}$  is high, and address must be valid prior to or coincident with  $\overline{CE}$  transition low.
7. Transition is measured  $\pm 200mV$  from steady state voltage prior to

change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

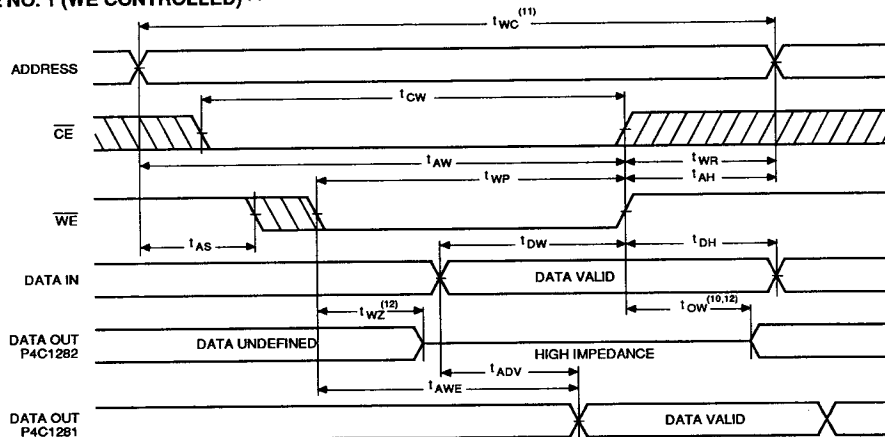
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

**AC CHARACTERISTICS—WRITE CYCLE**(V<sub>CC</sub> = 5V ± 10%, All Temperature Ranges)<sup>(2)</sup>

| Sym.             | Parameter                                  | -20* |     | -25 |     | -30 |     | -35 |     | -45 |     | -55 |     | Unit |
|------------------|--------------------------------------------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|                  |                                            | Min  | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| t <sub>WC</sub>  | Write Cycle Time                           | 16   |     | 20  |     | 25  |     | 30  |     | 40  |     | 50  |     | ns   |
| t <sub>CW</sub>  | Chip Enable Time to End of Write           | 15   |     | 20  |     | 25  |     | 30  |     | 35  |     | 40  |     | ns   |
| t <sub>AW</sub>  | Address Valid to End of Write              | 15   |     | 20  |     | 25  |     | 25  |     | 35  |     | 40  |     | ns   |
| t <sub>AS</sub>  | Address Set-up Time                        | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| t <sub>WP</sub>  | Write Pulse Width                          | 15   |     | 20  |     | 25  |     | 25  |     | 35  |     | 40  |     | ns   |
| t <sub>AH</sub>  | Address Hold Time from End of Write        | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| t <sub>WR</sub>  | Write Recovery Time                        | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| t <sub>DW</sub>  | Data Valid to End of Write                 | 12   |     | 13  |     | 15  |     | 15  |     | 20  |     | 25  |     | ns   |
| t <sub>DH</sub>  | Data Hold Time                             | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| t <sub>WZ</sub>  | Write Enable to Output in High Z (P4C1282) |      | 8   |     | 10  |     | 10  |     | 10  |     | 15  |     | 20  | ns   |
| t <sub>OW</sub>  | Output Active from End of Write (P4C1282)  | 2    |     | 2   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| t <sub>AWE</sub> | Write Enable to Data-out Valid (P4C1281)   |      | 18  |     | 20  |     | 25  |     | 30  |     | 35  |     | 40  | ns   |
| t <sub>ADV</sub> | Data-in Valid to Data-out Valid (P4C1281)  |      | 18  |     | 20  |     | 25  |     | 30  |     | 35  |     | 40  | ns   |

\*V<sub>CC</sub> = 5V ± 5% for -20

1549 Tbl 11

**WRITE CYCLE NO. 1 (WE CONTROLLED)<sup>(9)</sup>**

1549 06

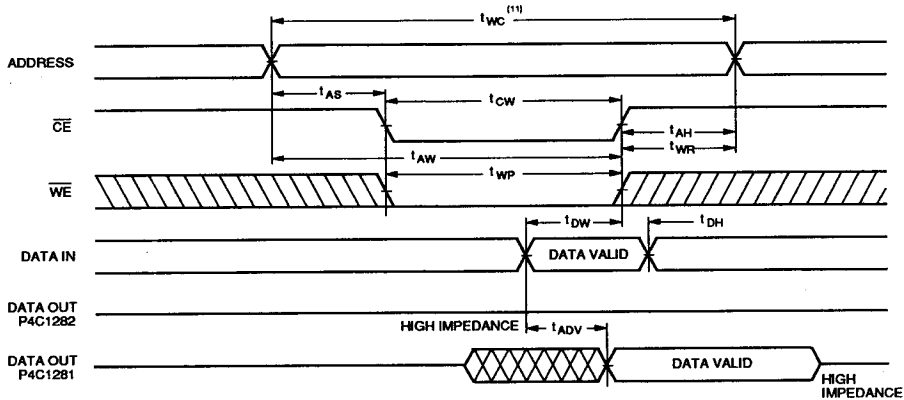
**Notes:**

9.  $\overline{CE}$  and  $\overline{WE}$  must be low for WRITE cycle.
10. If  $\overline{CE}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.

12. Transition is measured  $\pm 200\text{mV}$  from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.



## WRITE CYCLE NO. 2 (CE CONTROLLED) <sup>(9)</sup>



1549 07

## AC TEST CONDITIONS

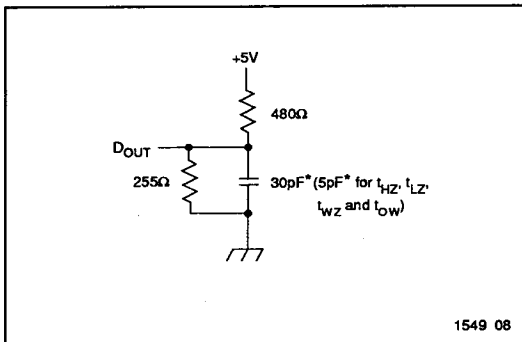
|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise and Fall Times     | 3ns                 |
| Input Timing Reference Level  | 1.5V                |
| Output Timing Reference Level | 1.5V                |
| Output Load                   | See Figures 1 and 2 |

1549 Tbl 12

## TRUTH TABLE P4C1281/L (P4C1282/L)

| Mode    | CE | WE | Output                   | Power   |
|---------|----|----|--------------------------|---------|
| Standby | H  | X  | High Z                   | Standby |
| Read    | L  | H  | D <sub>OUT</sub>         | Active  |
| Write   | L  | L  | D <sub>IN</sub> (High Z) | Active  |

1549 Tbl 13



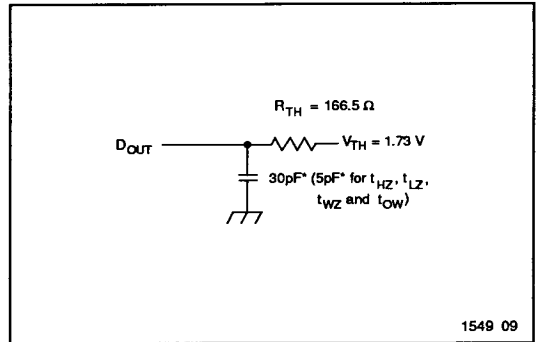
1549 08

Figure 1. Output Load

\* including scope and test fixture.

### Note:

Due to the ultra-high speed of the P4C1281/L and P4C1282/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>CC</sub> and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between

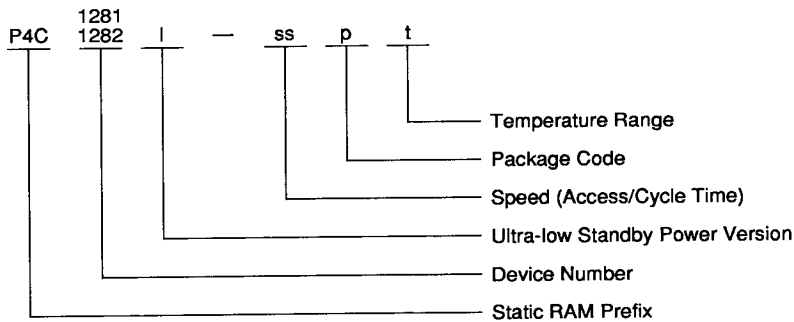


1549 09

Figure 2. Thevenin Equivalent

V<sub>CC</sub> and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D<sub>OUT</sub> to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



L = Ultra-low standby power designator L, if needed.  
ss = Speed (access/cycle time in ns), e.g., 25, 35  
p = Package code, i.e., P, J, C, L.  
t = Temperature range, i.e., C, M, MB.

1549 10

2

PACKAGE SUFFIX

| Package Suffix | Description                           |
|----------------|---------------------------------------|
| P              | Plastic DIP, 300 mil wide standard    |
| J              | Plastic SOJ, 300 mil wide standard    |
| C              | Sidebrazed DIP, 300 mil wide standard |
| L              | Leadless Chip Carrier (ceramic)       |

1549 Tbl 14

TEMPERATURE RANGE SUFFIX

| Temperature Range Suffix | Description                                     |
|--------------------------|-------------------------------------------------|
| C                        | Commercial Temperature Range, 0°C – +70°C.      |
| M                        | Military Temperature Range, –55°C – +125°C.     |
| MB                       | Mil. Temp. with MIL-STD-883C Class B compliance |

1549 Tbl 15

SELECTION GUIDE

The P4C1281/L and P4C1282/L are available in the following temperature, speed and package options.

| Temperature Range   | Speed          |  | 20    | 25     | 30     | 35     | 45     | 55     |
|---------------------|----------------|--|-------|--------|--------|--------|--------|--------|
|                     | Package        |  |       |        |        |        |        |        |
| Commercial          | Plastic DIP    |  | -20PC | -25PC  | -30PC  | -35PC  | N/A    | N/A    |
|                     | Plastic SOJ    |  | -20JC | -25JC  | -30JC  | -35JC  | N/A    | N/A    |
|                     | Sidebrazed DIP |  | -20CC | -25CC  | -30CC  | -35CC  | N/A    | N/A    |
|                     | LCC            |  | -20LC | -25LC  | -30LC  | -35LC  | N/A    | N/A    |
| Military Temp.      | Sidebrazed DIP |  | N/A   | -25CM  | -30CM  | -35CM  | -45CM  | -55CM  |
|                     | LCC            |  | N/A   | -25LM  | -30LM  | -35LM  | -45LM  | -55LM  |
| Military Processed* | Sidebrazed DIP |  | N/A   | -25CMB | -30CMB | -35CMB | -45CMB | -55CMB |
|                     | LCC            |  | N/A   | -25LMB | -30LMB | -35LMB | -45LMB | -55LMB |

\* Military temperature range with MIL-STD-883 Revision C, Class B processing.

N/A = Not available

Advance Information

1549 Tbl 16

TECHDOC 1549