FAIRCHILD SEMICONDUCTOR™

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FSTU6800A

10-Bit Bus Switch with Pre-Charged Outputs and −2V Undershoot Hardened Circuit (UHC™) Protection (Preliminary)

General Description

The Fairchild Switch FSTU6800A provides 10-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. Both the A Ports and the B Ports are "undershoot hardened" with UHC™ protection to support an extended input range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning on the switch. The device also precharges the B Port to a selectable bias voltage (BiasV) to minimize live insertion noise.

The device is organized as a 10-bit switch with a bus enable ($\overline{OE}$) signal. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and the B Port is precharged to BiasV through an equivalent 10-kΩ resistor.

Features

- 4Ω switch connection between two ports.
- Undershoot Hardened to -2.0V.
- Soft enable turn-on to minimize bus-to-bus charge sharing during enable.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Output precharge to minimize live insertion noise.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details.

Ordering Code:

Order Number	Package Number	Package Description
FSTU6800AWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
FSTU6800AQSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSTU6800AMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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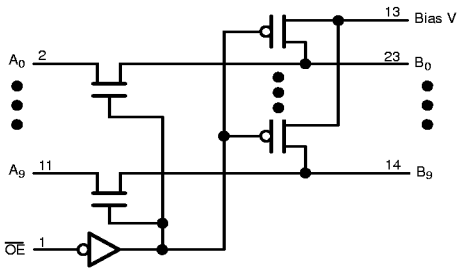
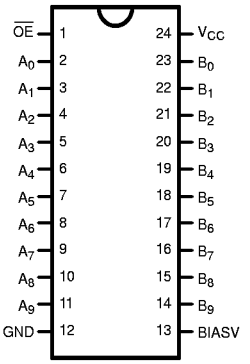
Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
A	Bus A
B	Bus B
BiasV	Bus B Voltage Bias

Truth Table

$\overline{OE}$	B_0–B_9	Function
L	A_0–A_9	Connect
H	BiasV	Precharge

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	0.5V to +7.0V
DC Switch Voltage (V_S)	–2.0V to +7.0V
Bias V Voltage Range	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}< 0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5V to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 nS/V to 5 nS/V
Switch I/O	0 nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18 mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, B = 0
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A ≤ V_{CC}, V_{IN} = V_{IH}
R_{ON}	Switch On Resistance (Note 4)	4.5		4	7	Ω	V_S = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_S = 0V, I_{IN} = 30 mA
		4.5		8	15	Ω	V_S = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_S = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_S = V_{CC} or GND, I_{OUT} = 0
Δ I_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	$\overline{OE}$ input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	$\overline{OE}$ = 0V, B = 0V, BiasV = 5.5V
I_{OZU}	Switch Undershoot Current	5.5			100	µA	I_{IN} = –20 mA, $\overline{OE}$ = 5.5V, V_{OUT} ≥ V_{IH}
V_{IKU}	Voltage Undershoot	5.5			–2.0	V	0.0 mA ≥ I_{IN} ≥ –50 mA, $\overline{OE}$ = 5.5V

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 – 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = Open	Figure 1 Figure 2
t_{PZH}	Output Enable Time	1.0	6.2		6.5	ns	V_I = Open BiasV = GND	Figure 1 Figure 2
t_{PZL}		1.0	6.2		6.5	ns	V_I = 7V BiasV = 3V	
t_{PHZ}	Output Disable Time	1.0	6.1		6.5	ns	V_I = Open BiasV = GND	Figure 1 Figure 2
t_{PLZ}		1.0	7.3		6.8	ns	V_I = 7V BiasV = 3V	

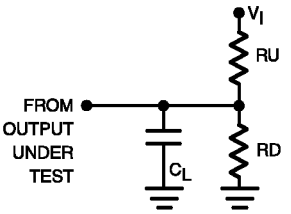
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω, RU = RD = 500 Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

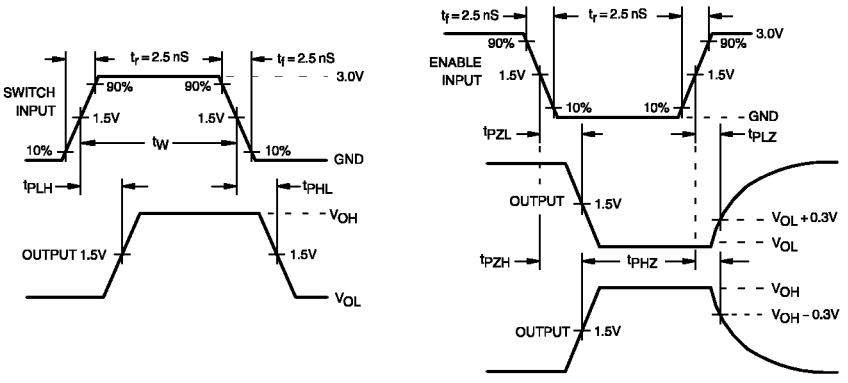
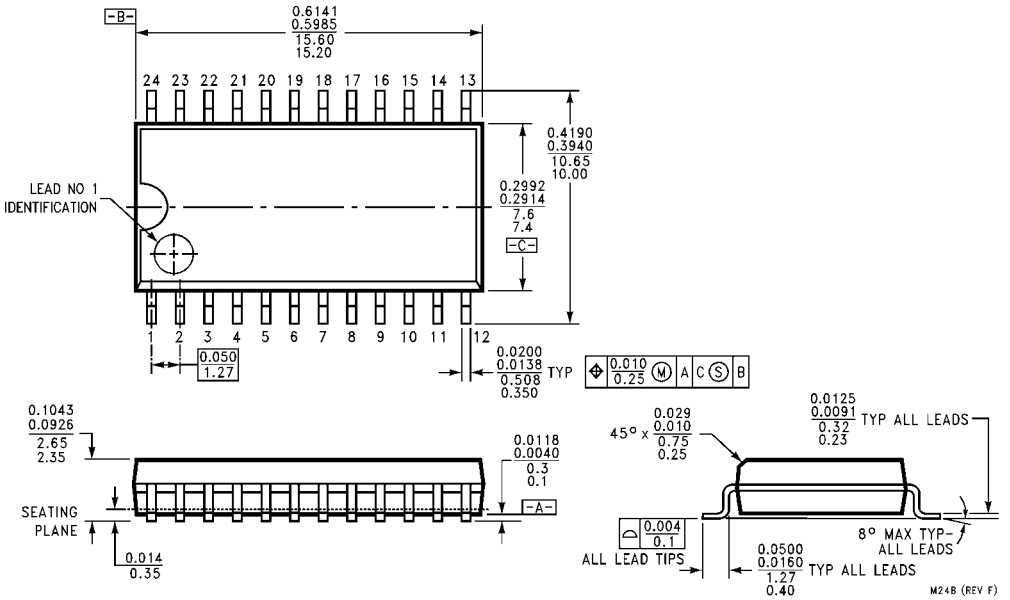
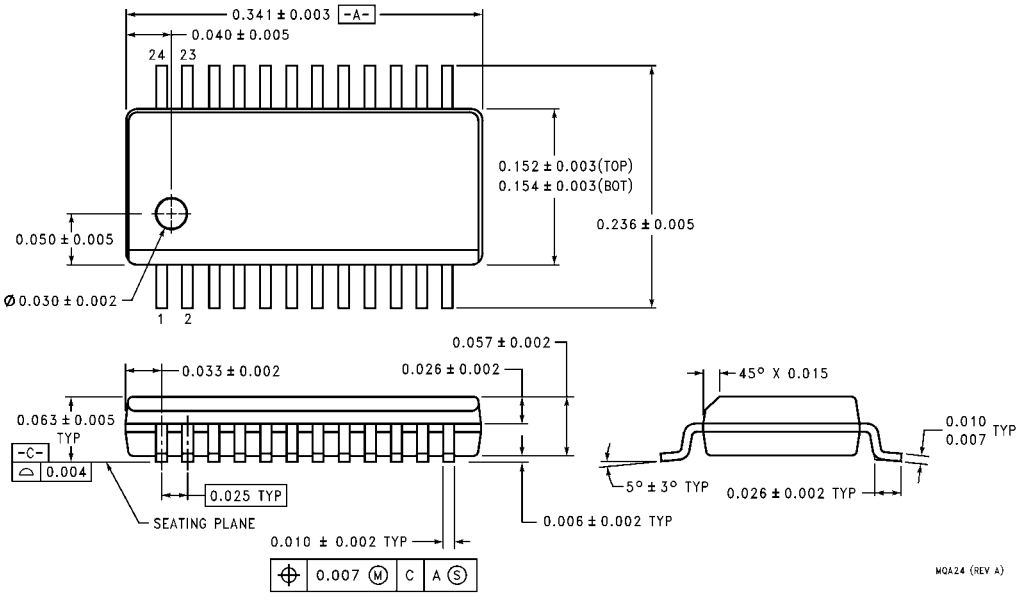


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

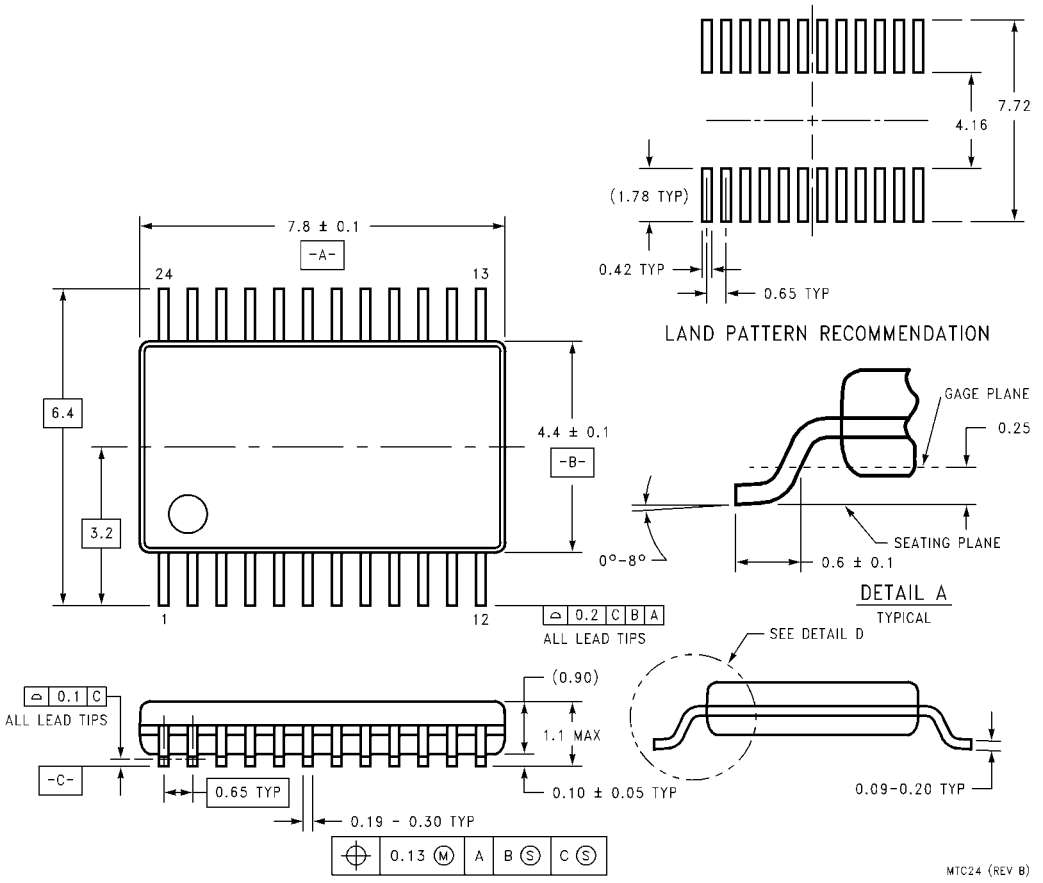


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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