

## 74VHCT573A

### Octal D-Type Latch with 3-STATE Outputs

#### General Description

The VHCT573A is an advanced high speed CMOS octal latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a Latch Enable input (LE) and an Output Enable input (OE). When the OE input is HIGH, the eight outputs are in a high impedance state.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. This device can be used to interface 3V to 5V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**Note 1:** Outputs in OFF-State.

#### Features

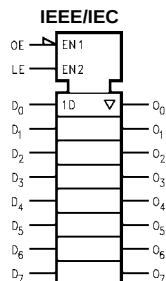
- High speed:  $t_{PD} = 7.7$  ns (typ) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{IH} = 2.0\text{V}$ ,  $V_{IL} = 0.8\text{V}$
- Power Down Protection is provided on all inputs and outputs
- Low Noise:  $V_{OLP} = 1.6\text{V}$  (max)
- Low Power Dissipation:  
 $I_{CC} = 4 \mu\text{A}$  (max) @  $T_A = 25^\circ\text{C}$
- Pin and function compatible with 74HCT573

#### Ordering Code:

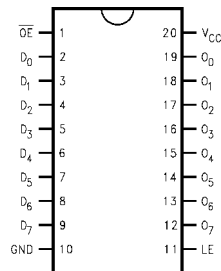
| Order Number  | Package Number | Package Description                                                         |
|---------------|----------------|-----------------------------------------------------------------------------|
| 74VHCT573AM   | M20B           | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  |
| 74VHCT573ASJ  | M20D           | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide       |
| 74VHCT573AMTC | MTC20          | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHCT573AN   | N20A           | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide      |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

#### Logic Symbol



#### Connection Diagram



## Pin Descriptions

| Pin Names                      | Description                 |
|--------------------------------|-----------------------------|
| D <sub>0</sub> –D <sub>7</sub> | Data Inputs                 |
| LE                             | Latch Enable Input          |
| $\overline{OE}$                | 3-STATE Output Enable Input |
| O <sub>0</sub> –O <sub>7</sub> | 3-STATE Outputs             |

## Truth Table

| Inputs          |    |   | Outputs        |
|-----------------|----|---|----------------|
| $\overline{OE}$ | LE | D | O <sub>n</sub> |
| L               | H  | H | H              |
| L               | H  | L | L              |
| L               | L  | X | O <sub>0</sub> |
| H               | X  | X | Z              |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

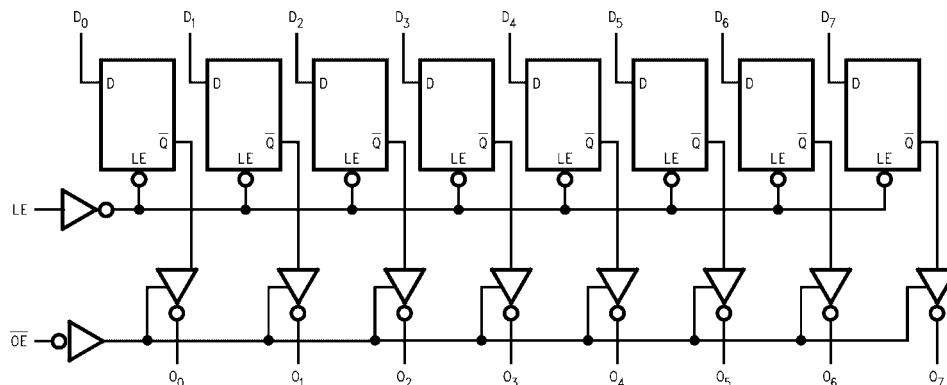
Z = High Impedance

## Functional Description

The VHCT573A contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on

the D inputs, a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 2)

|                                            |                          |
|--------------------------------------------|--------------------------|
| Supply Voltage ( $V_{CC}$ )                | –0.5V to +7.0V           |
| DC Input Voltage ( $V_{IN}$ )              | –0.5V to +7.0V           |
| DC Output Voltage ( $V_{OUT}$ )            |                          |
| (Note 3)                                   | –0.5V to $V_{CC} + 0.5V$ |
| (Note 4)                                   | –0.5V to +7.0V           |
| Input Diode Current ( $I_{IK}$ )           | –20 mA                   |
| Output Diode Current ( $I_{OK}$ ) (Note 5) | ±20 mA                   |
| DC Output Current ( $I_{OUT}$ )            | ±25 mA                   |
| DC $V_{CC}$ /GND Current ( $I_{CC}$ )      | ±75 mA                   |
| Storage Temperature ( $T_{STG}$ )          | –65°C to +150°C          |
| Lead Temperature ( $T_L$ )                 |                          |
| (Soldering, 10 seconds)                    | 260°C                    |

**Recommended Operating Conditions** (Note 6)

|                                         |                  |
|-----------------------------------------|------------------|
| Supply Voltage ( $V_{CC}$ )             | 4.5V to +5.5V    |
| Input Voltage ( $V_{IN}$ )              | 0V to +5.5V      |
| Output Voltage ( $V_{OUT}$ )            |                  |
| (Note 3)                                | 0V to $V_{CC}$   |
| (Note 4)                                | 0V to 5.5V       |
| Operating Temperature ( $T_{OPR}$ )     | –40°C to +85°C   |
| Input Rise and Fall Time ( $t_r, t_f$ ) |                  |
| $V_{CC} = 5.0V \pm 0.5V$                | 0 ns/V ~ 20 ns/V |

**Note 2:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 3:** HIGH or LOW state.  $I_{OUT}$  absolute maximum rating must be observed.

**Note 4:** When outputs are in OFF-State or when  $V_{CC} = 0V$ .

**Note 5:**  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$  (Outputs Active).

**Note 6:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

| Symbol    | Parameter                                    | $V_{CC}$<br>(V) | $T_A = 25^\circ C$ |      |       | $T_A = -40^\circ C$ to $+85^\circ C$ |      | Units | Conditions                                                 |
|-----------|----------------------------------------------|-----------------|--------------------|------|-------|--------------------------------------|------|-------|------------------------------------------------------------|
|           |                                              |                 | Min                | Typ  | Max   | Min                                  | Max  |       |                                                            |
| $V_{IH}$  | HIGH Level<br>Input Voltage                  | 4.5             | 2.0                |      |       | 2.0                                  |      | V     |                                                            |
|           |                                              | 5.5             | 2.0                |      |       | 2.0                                  |      |       |                                                            |
| $V_{IL}$  | LOW Level<br>Input Voltage                   | 4.5             |                    |      | 0.8   |                                      | 0.8  | V     |                                                            |
|           |                                              | 5.5             |                    |      | 0.8   |                                      | 0.8  |       |                                                            |
| $V_{OH}$  | HIGH Level<br>Output Voltage                 | 4.5             | 4.40               | 4.50 |       | 4.40                                 |      | V     | $V_{IN} = V_{IH}$ $I_{OH} = -50 \mu A$                     |
|           |                                              | 4.5             | 3.94               |      |       | 3.80                                 |      | V     | or $V_{IL}$ $I_{OH} = -8 mA$                               |
| $V_{OL}$  | LOW Level<br>Output Voltage                  | 4.5             |                    | 0.0  | 0.1   |                                      | 0.1  | V     | $V_{IN} = V_{IH}$ $I_{OL} = 50 \mu A$                      |
|           |                                              | 4.5             |                    |      | 0.36  |                                      | 0.44 | V     | or $V_{IL}$ $I_{OL} = 8 mA$                                |
| $I_{OZ}$  | 3-STATE Output<br>Off-State Current          | 5.5             |                    |      | ±0.25 |                                      | ±2.5 | μA    | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{OUT} = V_{CC}$ or GND |
| $I_{IN}$  | Input Leakage Current                        | 0 – 5.5         |                    |      | ±0.1  |                                      | ±1.0 | μA    | $V_{IN} = 5.5V$ or GND                                     |
| $I_{CC}$  | Quiescent Supply Current                     | 5.5             |                    |      | 4.0   |                                      | 40.0 | μA    | $V_{IN} = V_{CC}$ or GND                                   |
| $I_{CCT}$ | Maximum $I_{CC}$ /Input                      | 5.5             |                    |      | 1.35  |                                      | 1.50 | mA    | $V_{IN} = 3.4V$<br>Other Inputs = $V_{CC}$ or GND          |
| $I_{OFF}$ | Output Leakage Current<br>(Power Down State) | 0.0             |                    |      | 0.5   |                                      | 5.0  | μA    | $V_{OUT} = 5.5V$                                           |

**Noise Characteristics**

| Symbol                | Parameter                                | $V_{CC}$<br>(V) | $T_A = 25^\circ C$ |        | Units | Conditions    |
|-----------------------|------------------------------------------|-----------------|--------------------|--------|-------|---------------|
|                       |                                          |                 | Typ                | Limits |       |               |
| $V_{OLP}$<br>(Note 7) | Quiet Output Maximum Dynamic $V_{OL}$    | 5.0             | 1.2                | 1.6    | V     | $C_L = 50 pF$ |
| $V_{OLV}$<br>(Note 7) | Quiet Output Minimum Dynamic $V_{OL}$    | 5.0             | –1.2               | –1.6   | V     | $C_L = 50 pF$ |
| $V_{IHD}$<br>(Note 7) | Minimum HIGH Level Dynamic Input Voltage | 5.0             |                    | 2.0    | V     | $C_L = 50 pF$ |
| $V_{ILD}$<br>(Note 7) | Maximum LOW Level Dynamic Input Voltage  | 5.0             |                    | 0.8    | V     | $C_L = 50 pF$ |

**Note 7:** Parameter guaranteed by design.

## AC Electrical Characteristics

| Symbol            | Parameter                                         | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |     |      | T <sub>A</sub> = -40°C to +85°C |      | Units | Conditions             |                        |
|-------------------|---------------------------------------------------|------------------------|-----------------------|-----|------|---------------------------------|------|-------|------------------------|------------------------|
|                   |                                                   |                        | Min                   | Typ | Max  | Min                             | Max  |       |                        |                        |
| t <sub>PLH</sub>  | Propagation Delay Time<br>(LE to O <sub>n</sub> ) | 5.0 ± 0.5              |                       | 7.7 | 12.3 | 1.0                             | 13.5 | ns    |                        | C <sub>L</sub> = 15 pF |
| t <sub>PHL</sub>  |                                                   |                        |                       | 8.5 | 13.3 | 1.0                             | 14.5 |       |                        | C <sub>L</sub> = 50 pF |
| t <sub>PLH</sub>  | Propagation Delay Time<br>(D to O <sub>n</sub> )  | 5.0 ± 0.5              |                       | 5.1 | 8.5  | 1.0                             | 9.5  | ns    |                        | C <sub>L</sub> = 15 pF |
| t <sub>PHL</sub>  |                                                   |                        |                       | 5.9 | 9.5  | 1.0                             | 10.5 |       |                        | C <sub>L</sub> = 50 pF |
| t <sub>PZL</sub>  | 3-STATE Output                                    | 5.0 ± 0.5              |                       | 6.3 | 10.9 | 1.0                             | 12.5 | ns    | R <sub>L</sub> = 1 kΩ  | C <sub>L</sub> = 15 pF |
| t <sub>PZH</sub>  | Enable Time                                       |                        |                       | 7.1 | 11.9 | 1.0                             | 13.5 |       |                        | C <sub>L</sub> = 50 pF |
| t <sub>PLZ</sub>  | 3-STATE Output                                    | 5.0 ± 0.5              |                       | 8.8 | 11.2 | 1.0                             | 12.0 | ns    | R <sub>L</sub> = 1 kΩ  | C <sub>L</sub> = 50 pF |
| t <sub>PHZ</sub>  | Disable Time                                      |                        |                       |     |      |                                 |      |       |                        |                        |
| t <sub>OSLH</sub> | Output to Output                                  | 5.0 ± 0.5              |                       |     | 1.0  |                                 | 1.0  | ns    | (Note 8)               |                        |
| t <sub>OSHL</sub> | Skew                                              |                        |                       |     |      |                                 |      |       |                        |                        |
| C <sub>IN</sub>   | Input Capacitance                                 |                        |                       | 4   | 10   |                                 | 10   | pF    | V <sub>CC</sub> = Open |                        |
| C <sub>OUT</sub>  | Output Capacitance                                |                        |                       | 6   |      |                                 |      | pF    | V <sub>CC</sub> = 5.0V |                        |
| C <sub>PD</sub>   | Power Dissipation<br>Capacitance                  |                        |                       | 25  |      |                                 |      | pF    | (Note 9)               |                        |

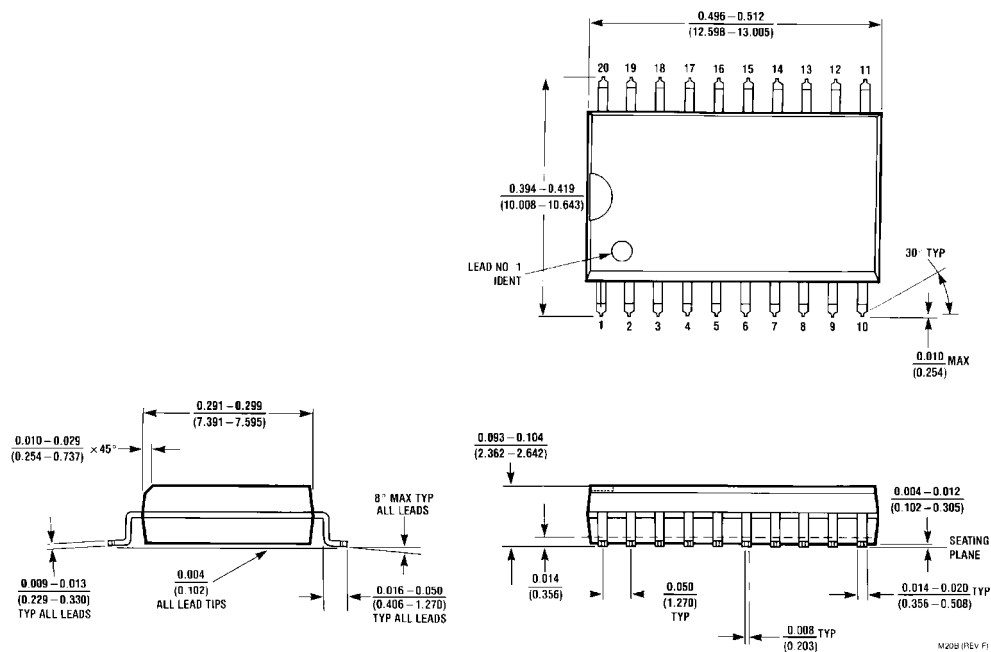
**Note 8:** Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLH</sub> max - t<sub>PLH</sub> min|; t<sub>OSHL</sub> = |t<sub>PHL</sub> max - t<sub>PHL</sub> min|

**Note 9:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (opr.) = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/8 (per F/F). The total C<sub>PD</sub> when n pcs. of the Latch operates can be calculated by the equation: C<sub>PD</sub>(total) = 14 + 13n.

## AC Operating Requirements

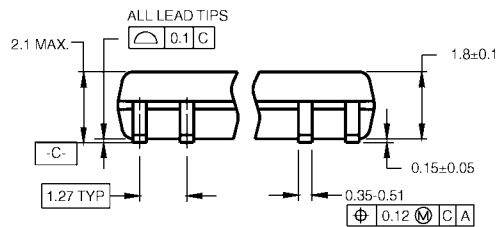
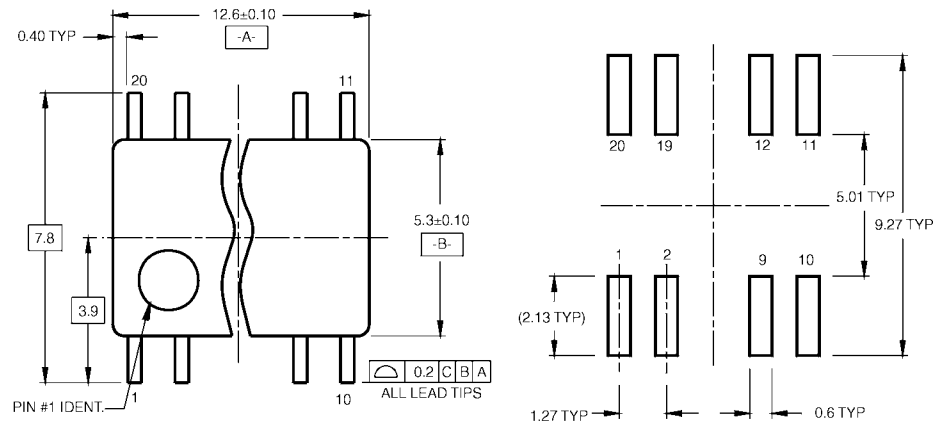
| Symbol            | Parameter                | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |     |     | T <sub>A</sub> = -40°C to +85°C |     | Units |
|-------------------|--------------------------|------------------------|-----------------------|-----|-----|---------------------------------|-----|-------|
|                   |                          |                        | Min                   | Typ | Max | Min                             | Max |       |
| t <sub>W(H)</sub> | Minimum Pulse Width (LE) | 5.0 ± 0.5              |                       | 6.5 |     | 8.5                             |     | ns    |
| t <sub>S</sub>    | Minimum Setup Time       | 5.0 ± 0.5              |                       | 1.5 |     | 1.5                             |     | ns    |
| t <sub>H</sub>    | Minimum Hold Time        | 5.0 ± 0.5              |                       | 3.5 |     | 3.5                             |     | ns    |

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

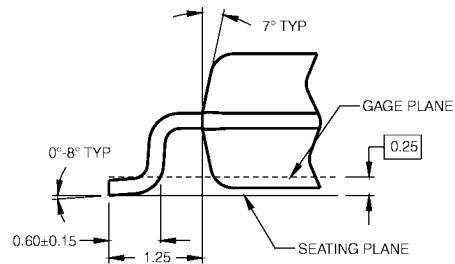


DIMENSIONS ARE IN MILLIMETERS

## NOTES:

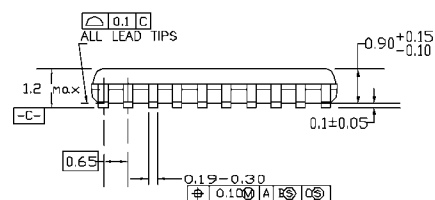
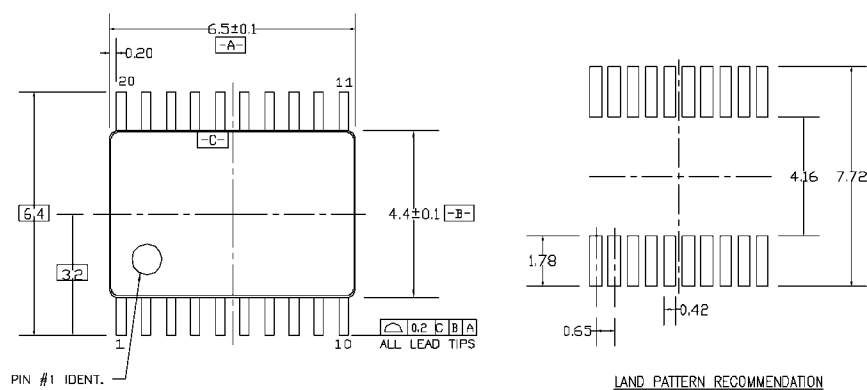
- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

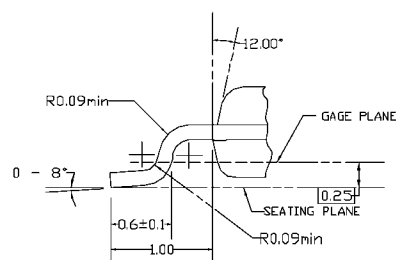
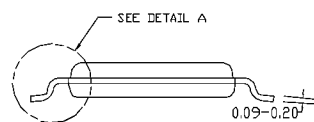


DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

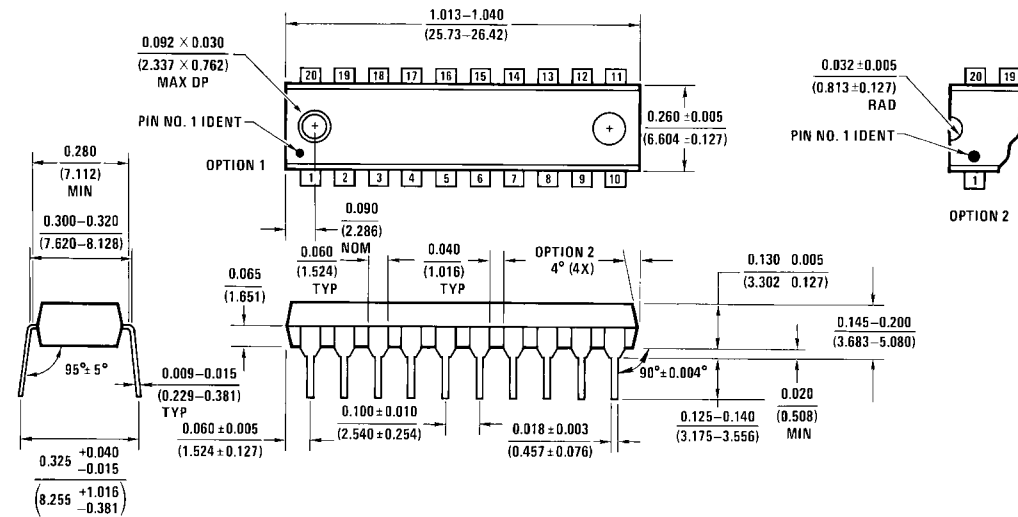
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,  
REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,  
AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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