

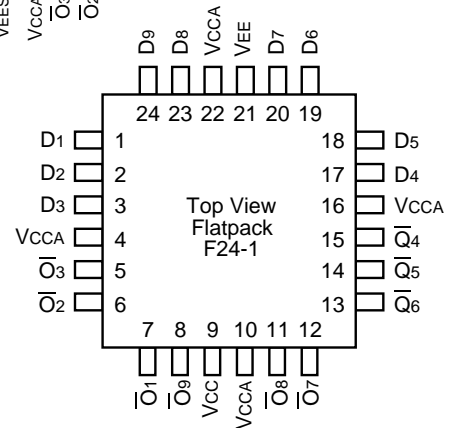
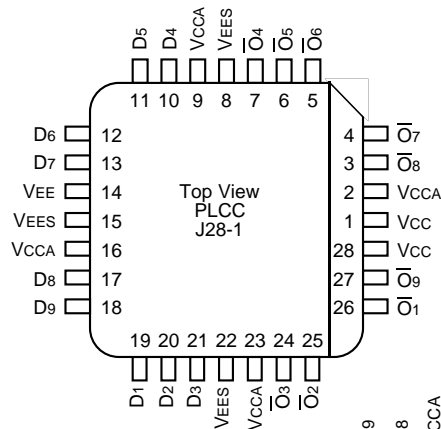
FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

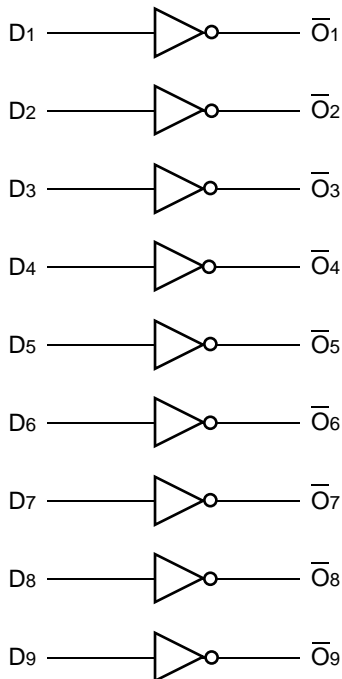
DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

| Pin | Function |
|-----------------------|----------------------|
| D1 – D9 | Data Inputs |
| $\bar{Q}1 – \bar{Q}9$ | Data Outputs |
| VEES | VEE Substrate |
| VCCA | Vcco for ECL Outputs |

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|-----------------|----------------------|------|------|------|------|--------------------------|
| I _{IH} | Input HIGH Current | — | — | 200 | μA | $V_{IN} = V_{IH} (Max.)$ |
| I _{EE} | Power Supply Current | -55 | -41 | -25 | mA | Inputs Open |

AC ELECTRICAL CHARACTERISTICS**CERPACK**

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +85°C | | Unit | Condition |
|--------------------------------------|--|----------------------|------|------------------------|------|------------------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay ⁽¹⁾ Data to Output | 300 | 800 | 300 | 800 | 300 | 800 | ps | |
| t _{TLH} t _{THL} | Transition Time ⁽¹⁾ 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |
| t _{S, G-G} | Skew, Gate-to-Gate | — | 200 | — | 200 | — | 200 | ps | |

NOTE:

- Reference figures 1 and 2

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +85°C | | Unit | Condition |
|--------------------------------------|--|----------------------|------|------------------------|------|------------------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay ⁽¹⁾ Data to Output | 300 | 700 | 300 | 700 | 300 | 700 | ps | |
| t _{TLH} t _{THL} | Transition Time ⁽¹⁾ 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |
| t _{S, G-G} | Skew, Gate-to-Gate | — | 200 | — | 200 | — | 200 | ps | |

NOTE:

- Reference figures 1 and 2

TEST CIRCUITRY⁽¹⁾

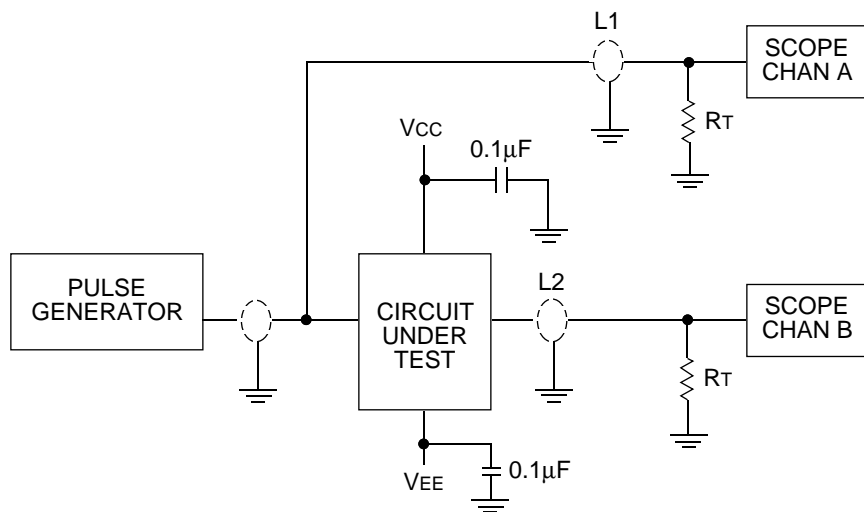


Figure 1. AC Test Circuit

NOTE:

- 1. VCC, VCCA = +2V, VEE = -2.5V.
- L1 and L2 = equal length 50Ω impedance lines.
- RT = 50Ω terminator internal to scope.
- Decoupling 0.1µF from GND to Vcc and VEE.
- All unused outputs are loaded with 50Ω to GND.
- CL = Fixture and stray capacitance ≤ 3pF.

SWITCHING WAVEFORMS

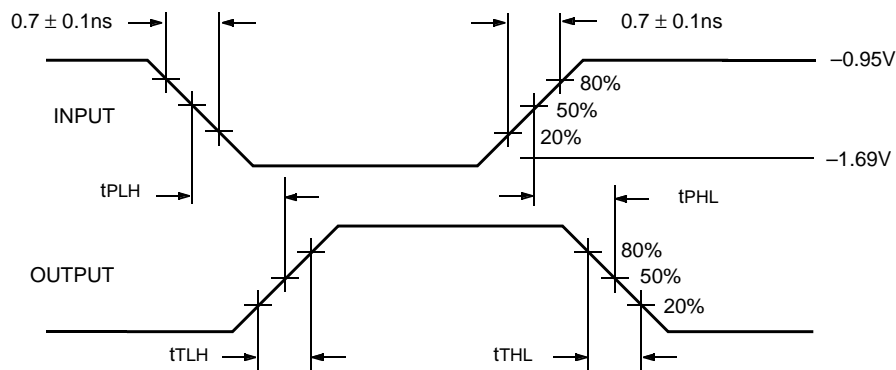


Figure 2. Propagation Delay and Transition Times

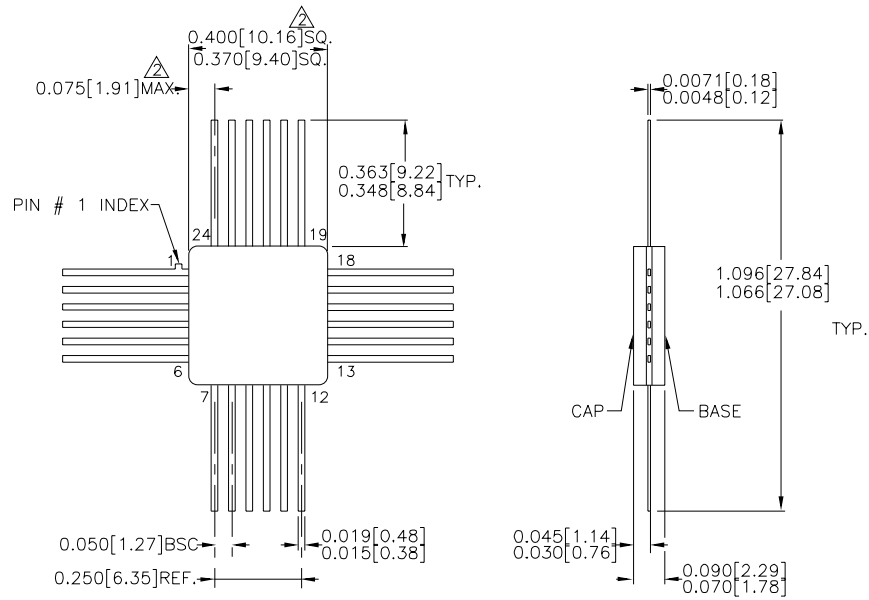
NOTE:

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

PRODUCT ORDERING CODE

| Ordering Code | Package Type | Operating Range |
|---------------|--------------|-----------------|
| SY100S321FC | F24-1 | Commercial |
| SY100S321JC | J28-1 | Commercial |
| SY100S321JCTR | J28-1 | Commercial |

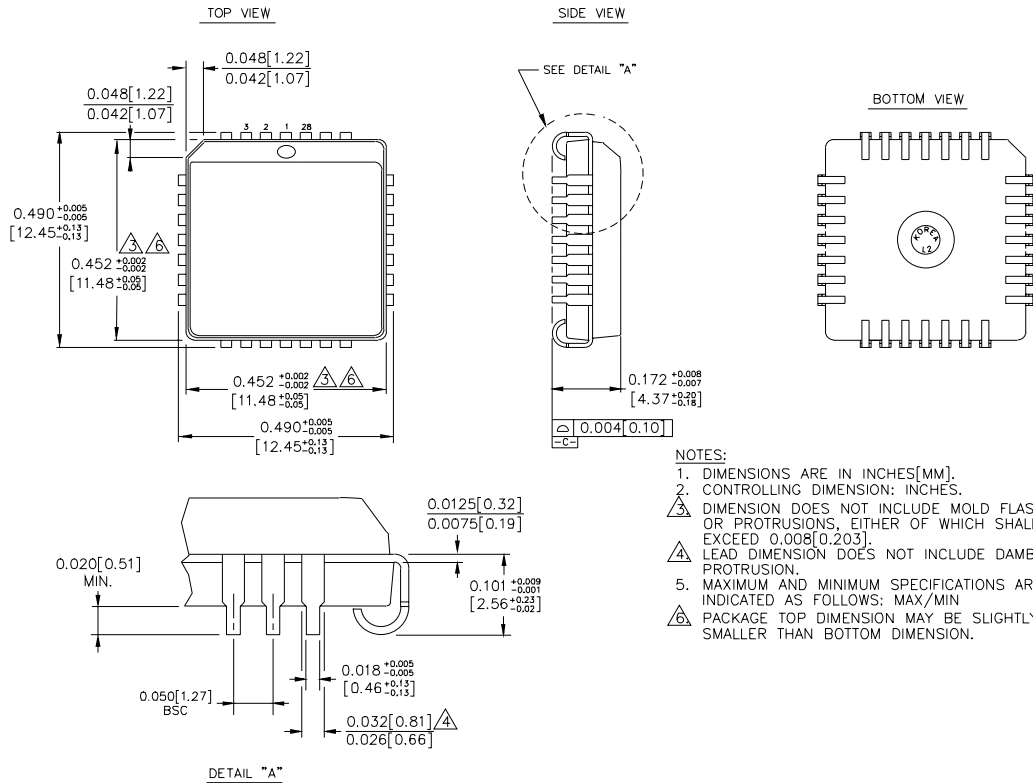
24 LEAD CERPACK (F24-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 - △ THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

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