MC10EP31, MC100EP31

3.3V / 5V ECL D Flip-Flop with Set and Reset

The MC10/100EP31 is a D flip–flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip–flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

The 100 Series contains temperature compensation.
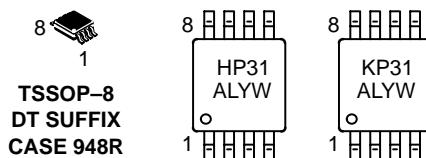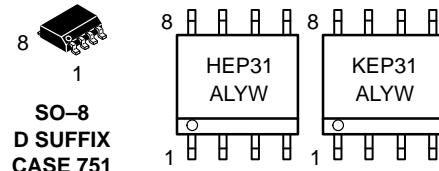
- 340 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.0 V to –5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}

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MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751

HEP31
ALYW

KEP31
ALYW

TSSOP–8
DT SUFFIX
CASE 948R

HP31
ALYW

KP31
ALYW

H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP31D	SO–8	98 Units/Rail
MC10EP31DR2	SO–8	2500 Tape & Reel
MC100EP31D	SO–8	98 Units/Rail
MC100EP31DR2	SO–8	2500 Tape & Reel
MC10EP31DT	TSSOP–8	100 Units/Rail
MC10EP31DTR2	TSSOP–8	2500 Tape & Reel
MC100EP31DT	TSSOP–8	100 Units/Rail
MC100EP31DTR2	TSSOP–8	2500 Tape & Reel

MC10EP31, MC100EP31
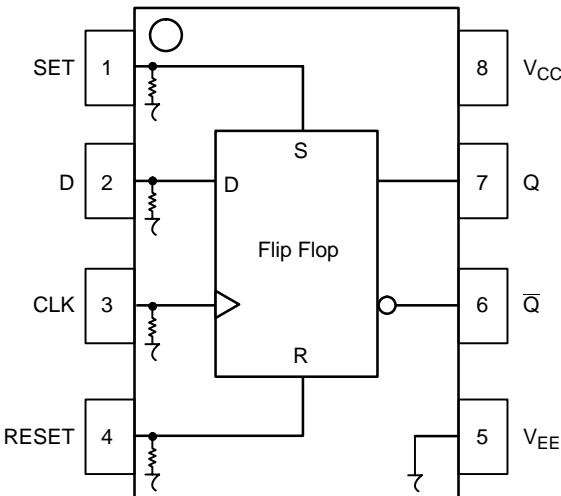
Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

PIN	FUNCTION
CLK*	ECL Clock Inputs
Reset*	ECL Asynchronous Reset
Set*	ECL Asynchronous Set
D*	ECL Data Input
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

TRUTH TABLE

D	SET	RESET	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	UNDEF

Z = LOW to HIGH Transition

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1.)		Level 1
Flammability Rating		UL–94 code V–0 A 1/8"
Oxygen Index		28 to 34
Transistor Count		75 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

MC10EP31, MC100EP31

10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 4.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
4. All loading with 50 ohms to V_{CC}−2.0 volts.

10EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 5.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 6.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 6.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single Ended)	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
6. All loading with 50 ohms to V_{CC}−2.0 volts.

10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 7.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 8.)	−1135	−1060	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 8.)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single Ended)	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single Ended)	−1935		−1610	−1870		−1545	−1810		−1485	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
7. Input and output parameters vary 1:1 with V_{CC}.
8. All loading with 50 ohms to V_{CC}−2.0 volts.

MC10EP31, MC100EP31

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 9.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 10.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 10.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
9. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
10. All loading with 50 ohms to V_{CC}−2.0 volts.

100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 11.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 12.)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 12.)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
12. All loading with 50 ohms to V_{CC}−2.0 volts.

100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 13.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 14.)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 14.)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
13. Input and output parameters vary 1:1 with V_{CC}.
14. All loading with 50 ohms to V_{CC}−2.0 volts.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.0 V to –5.5 V   or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 15.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. F$_{max}$/JITTER)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	CLK to Q, $\overline{Q}$	250	330	400	270	340	410	300	370	440	
	S, R to Q, $\overline{Q}$	300	380	450	330	400	470	360	430	500	
t_{RR}	Set/Reset Recovery	225			225			225			ps
t_S t_H	Setup Time Hold Time	100 150			100 150			100 150			ps
t_{PW}	Minimum Pulse width SET, RESET	550	450		550	450		550	450		ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 2. F$_{max}$/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	50	120	180	60	130	200	70	150	220	ps

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.

Figure 2. F$_{max}$/Jitter

$$V_{TT} = V_{CC} - 2.0\ V$$
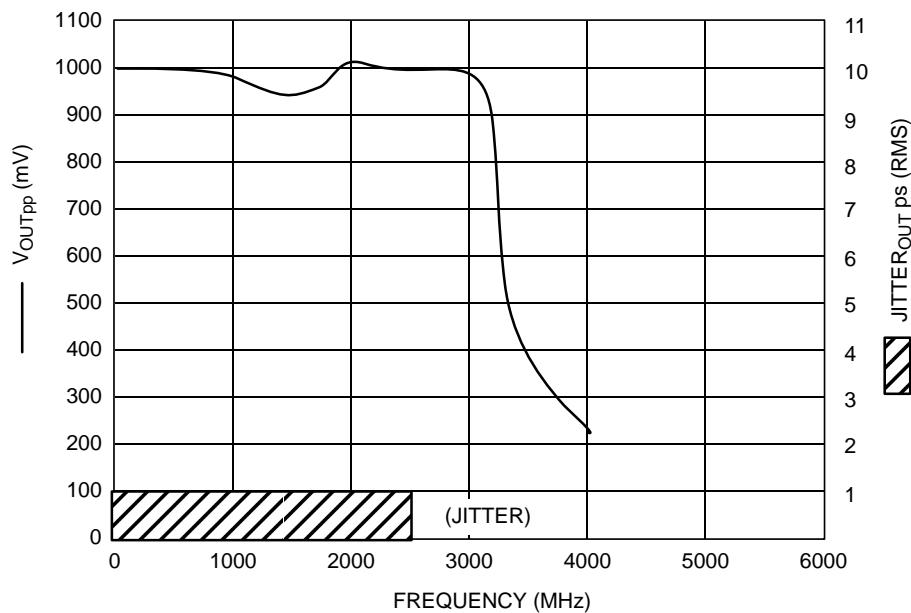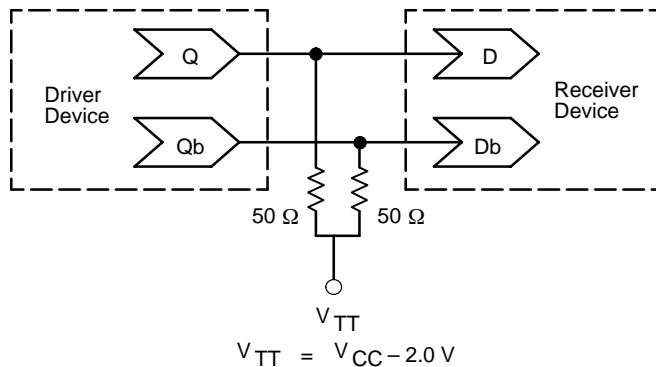
**Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)**

Resource Reference of Application Notes
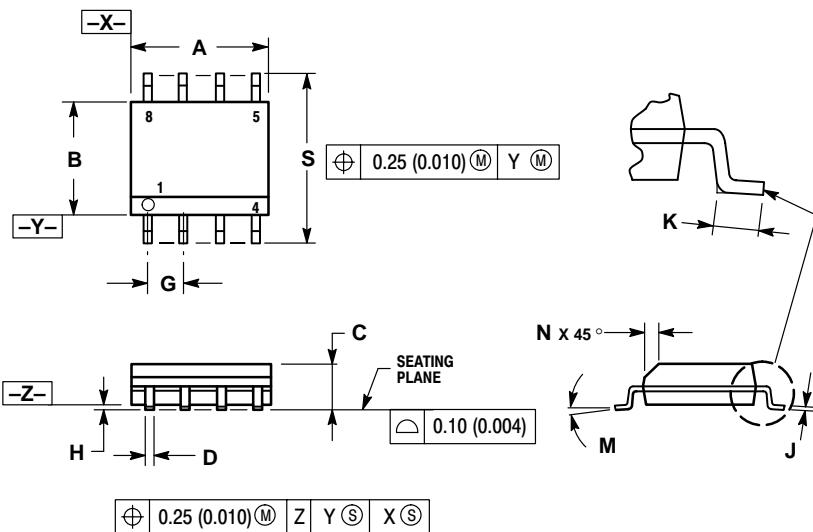
AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8009	–	ECLinPS Plus Spice I/O Model Kit
AND8020	–	Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.
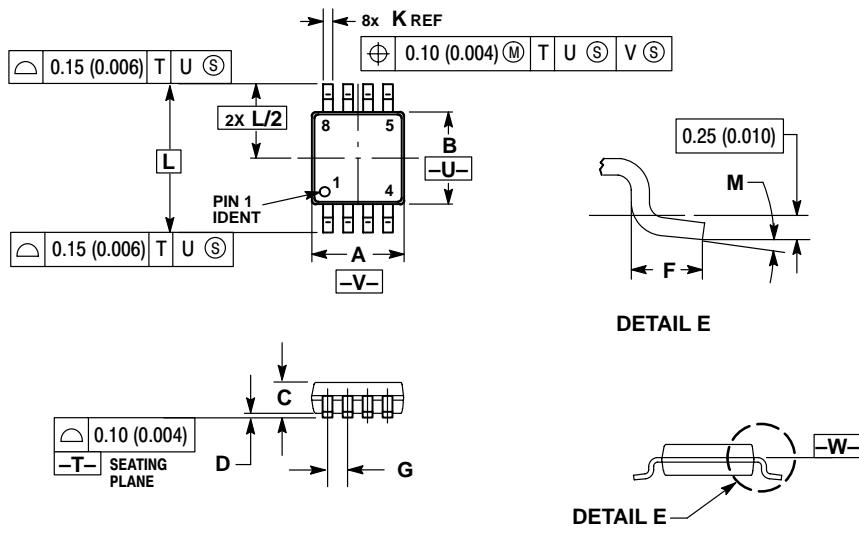
PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE W

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

DETAIL E