

SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 – MARCH 1985 – REVISED MARCH 1988

'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level (\overline{CS}) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

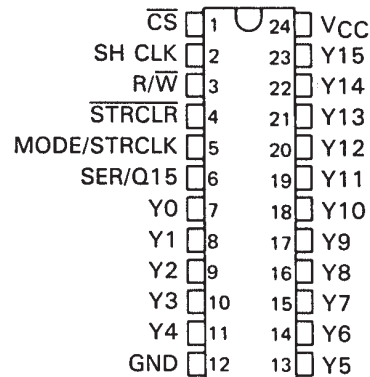
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

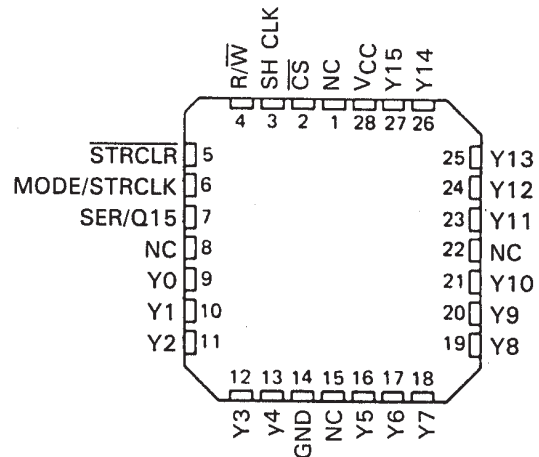
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS673 . . . J OR W PACKAGE SN74LS673 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS673 . . . FK PACKAGE (TOP VIEW)

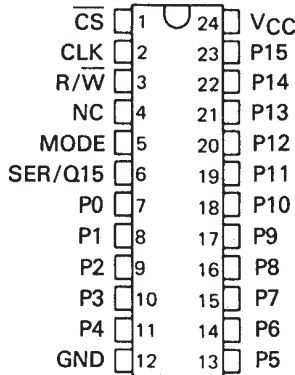


NC—No internal connection

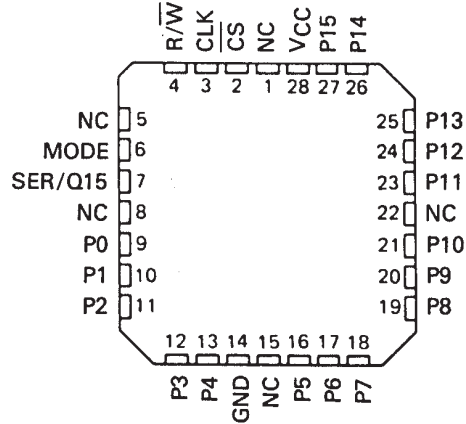
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SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . FK PACKAGE
(TOP VIEW)



'LS673
FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
CS	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
CS	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

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logic symbols†

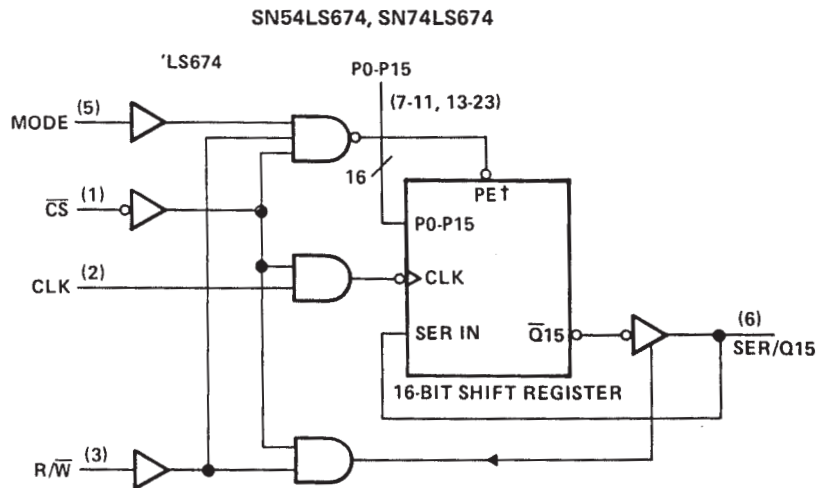
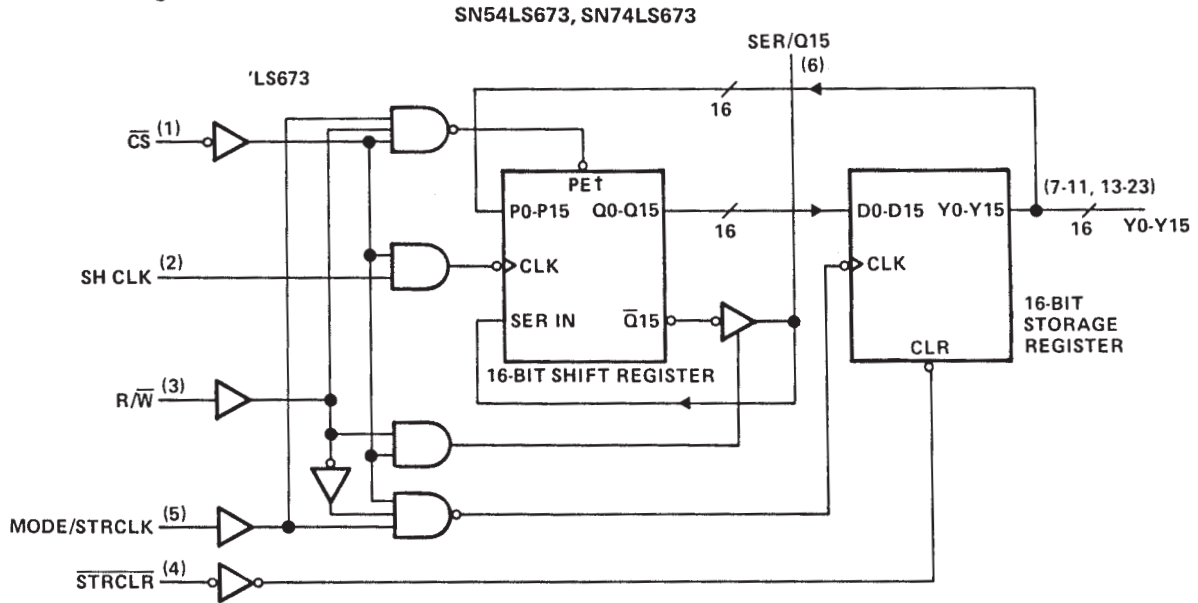


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

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functional block diagrams



†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

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16-BIT SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT
			MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.7		0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5		-1.5	V
V _{OH}	High-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,		2.4	3.1	V
		Y0 thru Y15¶	V _{IL} = V _{ILmax} , I _{OH} = MAX		2.5	3.4	
V _{OL}	Low-level output voltage	SER/Q15	V _{CC} = MIN, V _{IH} = 2 V,	I _{OL} = 12 mA	0.25	0.4	V
				I _{OL} = 24 mA		0.35	
		Y0 thru Y15¶	V _{IL} = V _{ILmax}	I _{OL} = 4 mA	0.25	0.4	
				I _{OL} = 8 mA		0.35	
I _{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 2.7 V	40		40	μA
I _{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 0.4 V	-0.4		-0.4	mA
I _I	Input current at maximum input voltage	SER/Q15	V _{CC} = MAX	V _I = 5.5 V		0.1	mA
		Others		V _I = 7 V		0.1	
I _{IH}	High-level input current	SER/Q15	V _{CC} = MAX, V _I = 2.7 V			40	μA
		Others				20	
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
I _{OS}	Short-circuit output current§	SER/Q15	V _{CC} = MAX		-30	-130	mA
		Y0 thru Y15¶			-20	-100	
I _{CC}	Supply current	'LS673	V _{CC} = MAX		50	80	mA
		'LS674			25	40	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673		'LS674		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FROM	TO	FROM	TO					
f _{max}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF	20	28		MHz
t _{PHL}	STRCLR	Y0 thru Y15			R _L = 2 kΩ, C _L = 15 pF		25	40	ns
t _{PLH}	MODE/ STRCLK	Y0 thru Y15					28	45	
t _{PHL}							30	45	
t _{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R _L = 667 Ω, C _L = 45 pF		21	33	ns
t _{PHL}							26	40	
t _{PZH}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 45 pF		30	45	ns
t _{PZL}							30	45	
t _{PHZ}	CS, R/W	SER/Q15	CS, R/W	SER/Q15	R _L = 667 Ω, C _L = 5 pF		25	40	ns
t _{PLZ}							25	40	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88602013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8860201JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860201KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8860201LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-88607013A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8860701JA	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
5962-8860701KA	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS673N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS673NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS674DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS674N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free	CU NIPDAU	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
(RoHS)								
SN74LS674NE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673FK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS673W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674FK	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674J	ACTIVE	CDIP	J	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54LS674W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

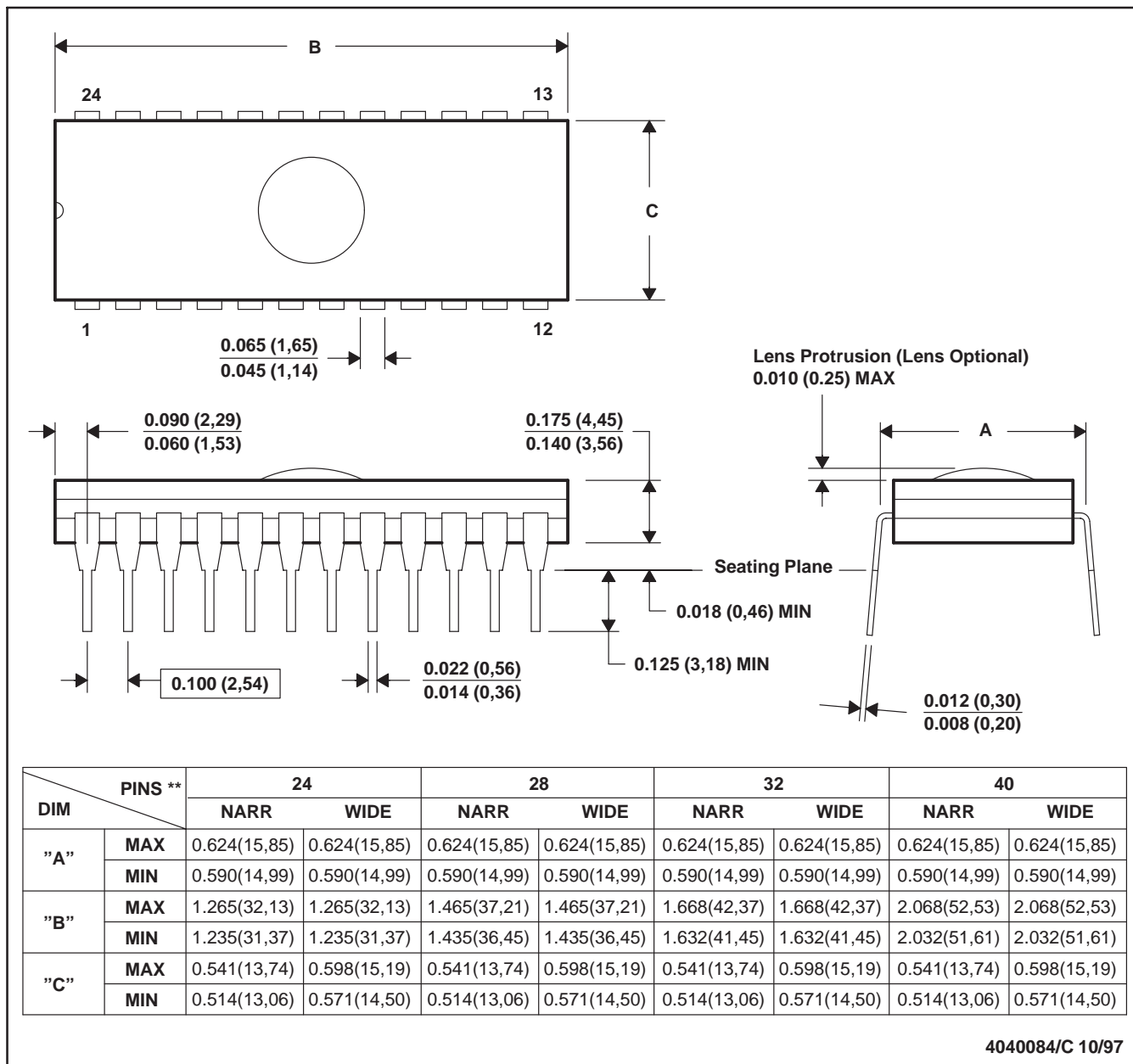
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J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

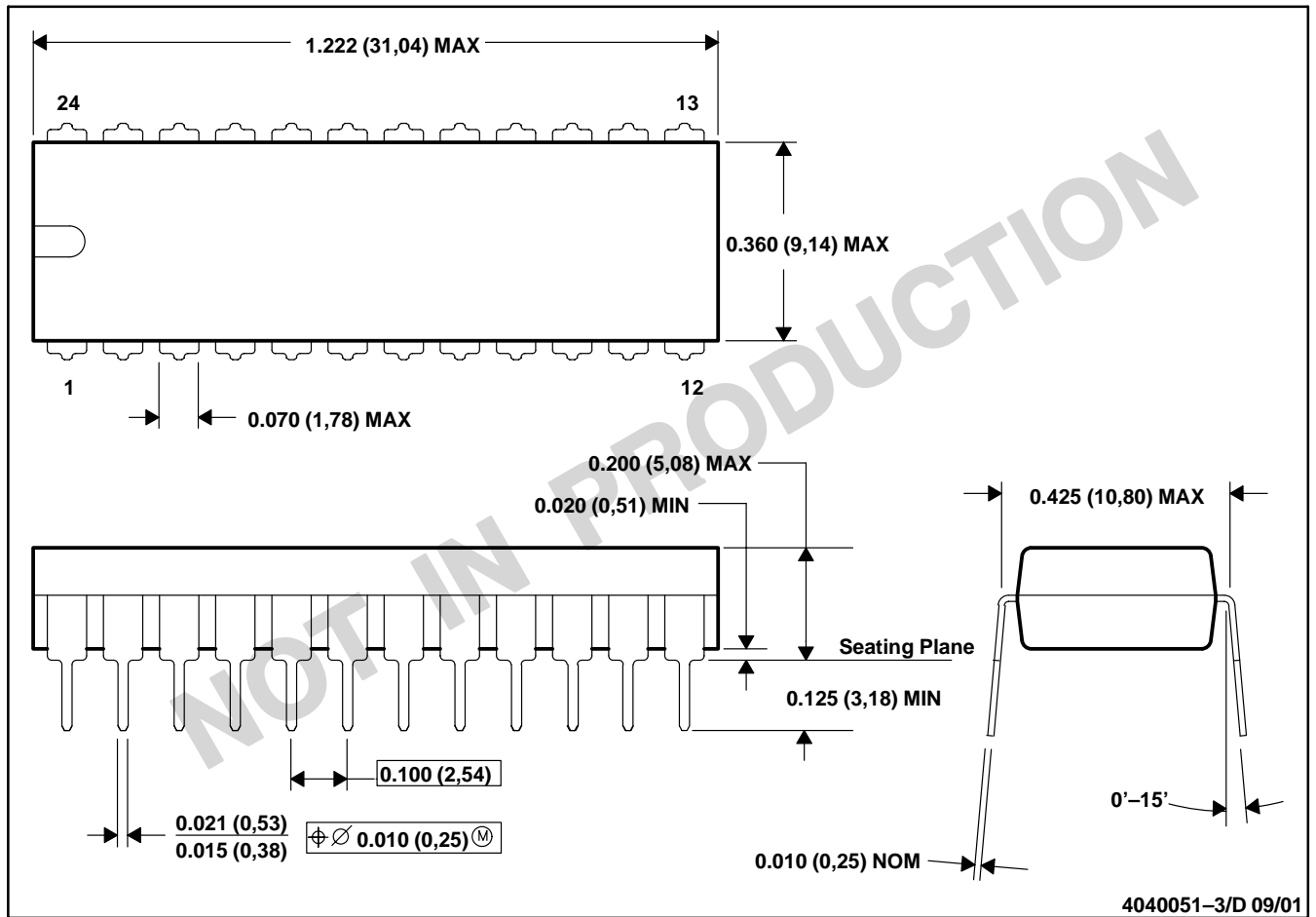
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-010

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

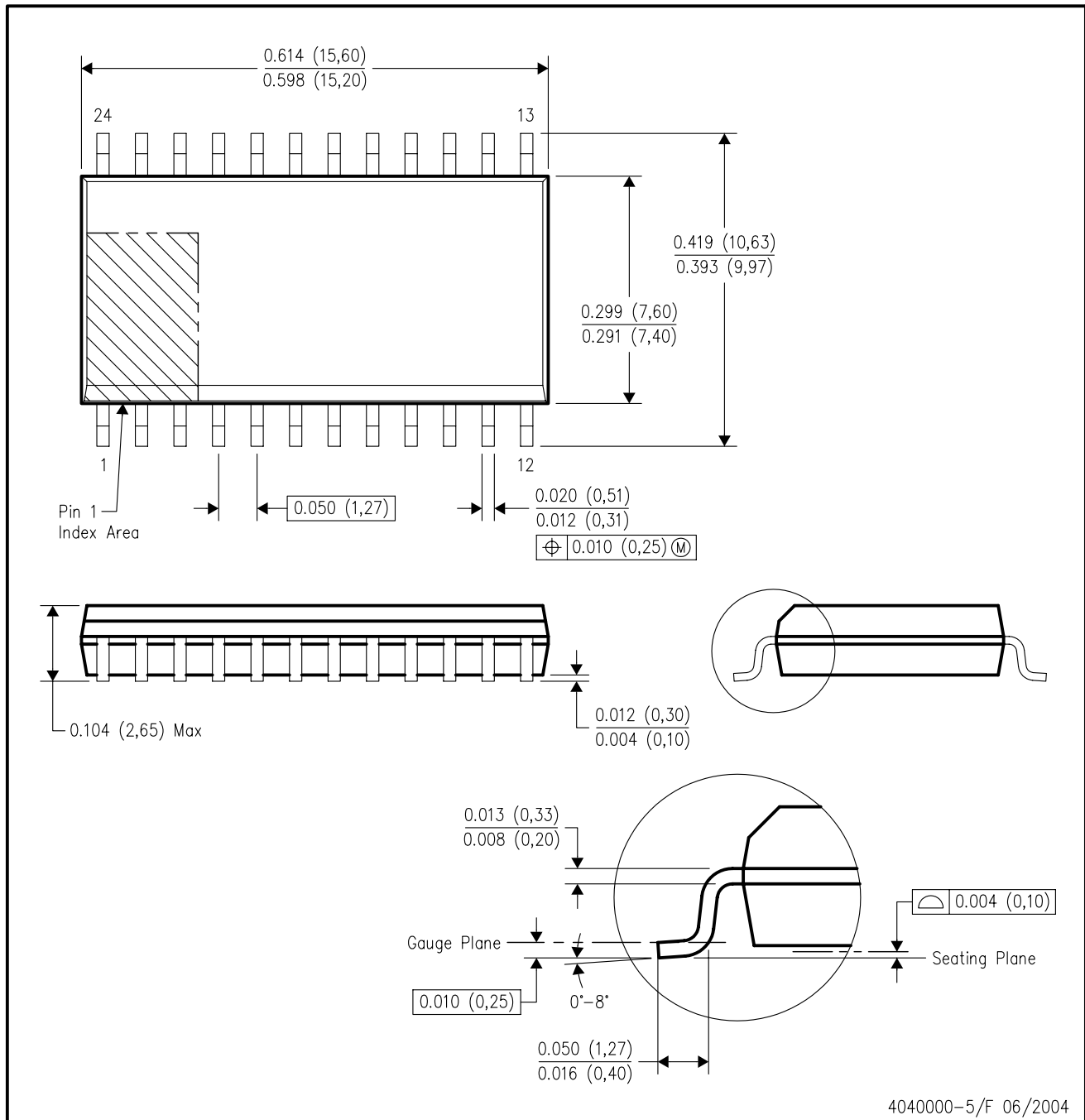
24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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