

**REVISIONS**

| LTR | DESCRIPTION   | DATE (YR-MO-DA) | APPROVED       |
|-----|---|-----------------|----------------|
| A   | Convert to approved source format   | 82-06-04        | N.A. Hauck     |
| B   | Addition of MIL spec replacement numbers plus part number corrections, editorial changes  | 82-08-11        | N.A. Hauck     |
| C   | Added 1 vendor, FSCM 27014  | 83-09-05        | N.A. Hauck     |
| D   | Removed 1 vendor; FSCM 27014 for device 02. Inactivate device 01, case C only for new design. Removed 1 vendor; FSCM 31019 for device 01, case D. | 85-01-04        | N.A. Hauck     |
| E   | Technical and editorial changes throughout. Changed to SMD format. Added device type 03.  | 94-02-17        | M. L. Poelking |

THE FRONT PAGE OF THIS DRAWING HAS BEEN REPLACED

**CURRENT CAGE CODE 67268**

|  |                                   |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
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| REV  |                                   |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
| SHEET  |                                   |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
| REV  |                                   |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
| SHEET  |                                   |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
| REV STATUS OF SHEETS   | REV                               | E | E | E | E | E | E | E | E | E | E   | E                         |              |   |  |  |  |  |  |  |
|  | SHEET                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |   |                           |              |   |  |  |  |  |  |  |
| PMIC N/A   | PREPARED BY<br>A.J. Foley         |   |   |   |   |   |   |   |   |   | DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444         |                           |              |   |  |  |  |  |  |  |
| <b>STANDARDIZED MILITARY DRAWING</b><br><br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br><br>AMSC N/A | CHECKED BY<br>C.R. Jackson        |   |   |   |   |   |   |   |   |   | MICROCIRCUIT, DIGITAL, CMOS DUAL D FLIP-FLOP MONOLITHIC SILICON |                           |              |   |  |  |  |  |  |  |
|  | APPROVED BY<br>N.A. Hauck         |   |   |   |   |   |   |   |   |   |   |                           |              |   |  |  |  |  |  |  |
|  | DRAWING APPROVAL DATE<br>79-05-14 |   |   |   |   |   |   |   |   |   | SIZE<br><b>A</b>  | CAGE CODE<br><b>14933</b> | <b>79011</b> |   |  |  |  |  |  |  |
|  | REVISION LEVEL<br>E               |   |   |   |   |   |   |   |   |   | SHEET   | 1                         | OF           | 9 |  |  |  |  |  |  |

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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

5962-E426-93

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u> |
|--------------------|-----------------------|-------------------------|
| 01                 | 4013B                 | Dual D type flip-flop   |
| 02                 | 4013B                 | Dual D type flip-flop   |
| 03                 | 14013B                | Dual D type flip-flop   |

1.2.2 Case outline(s). The case outline shall be as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|----------------------|
| C                     | CDIP2-T14 or GDIP1-T14        | 14               | Dual-in-line package |
| D                     | CDFP2-F14 or GDFP1-F14        | 14               | flat-package         |

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

|  |                                 |
|--|---------------------------------|
| Supply voltage range ( $V_{DD}$ ) - - - - -                  | -0.5 V dc to +18 V dc           |
| Input voltage range - - - - -                                | -0.5 V dc to $V_{DD}$ +0.5 V dc |
| Storage temperature range- - - - -                           | -65°C to +150°C                 |
| Maximum power dissipation per device ( $P_D$ ) <u>1/</u> - - | 500 mW <u>2/</u>                |
| Lead temperature (soldering 10 seconds)- - - - -             | +300°C                          |
| Thermal resistance, junction to case ( $\theta_{JC}$ ) - - - | See MIL-STD-1835                |
| Junction temperature ( $T_J$ )- - - - -                      | +175°C                          |

1.4 Recommended operating conditions.

|  |                       |
|--|-----------------------|
| Supply voltage - - - - -                   | +3.0 V dc to +15 V dc |
| Case operating temperature range - - - - - | -55°C to +125°C       |

1/ Must withstand the added  $P_D$  due to short circuit test, e.g.,  $I_{OS}$ .

2/ For  $T_C = +100^\circ\text{C}$  to  $+125^\circ\text{C}$ , derate linearly at 12 mW/°C to 200 mW.

|   |                  |                            |            |
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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards and bulletin. Unless otherwise specified, the following specifications standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of specifications, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883(see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.6 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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TABLE I. Electrical characteristics.

| Test   | Symbol            | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ 125°C<br>Unless otherwise specified  | Device<br>type   | Group A<br>subgroups | Limits                |                      | Units |     |     |
|--|-------------------|---|--|----------------------|-----------------------|----------------------|-------|-----|-----|
|  |                   |   |  |                      | Min                   | Max                  |       |     |     |
| High-level output<br>voltage                             | V <sub>OH</sub>   | V <sub>DD</sub> = 5 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub><br>V <sub>DD</sub> = 10 V<br>V <sub>DD</sub> = 15 V   | ALL  | 1, 2, 3              | 4.95<br>9.95<br>14.95 |                      | V     |     |     |
| Low-level output<br>voltage                              | V <sub>OL</sub>   | V <sub>DD</sub> = 5 V, V <sub>IN</sub> = 0 V or V <sub>DD</sub><br>V <sub>DD</sub> = 10 V<br>V <sub>DD</sub> = 15 V   | ALL  | 1, 2, 3              |                       | 0.05<br>0.05<br>0.05 | V     |     |     |
| High-level input<br>voltage                              | V <sub>IH</sub>   | V <sub>DD</sub> = 5 V, V <sub>O</sub> = 0.5 or 4.5 V<br>V <sub>DD</sub> = 10 V, V <sub>O</sub> = 1.0 or 9.0 V<br>V <sub>DD</sub> = 15 V, V <sub>O</sub> = 1.5 or 13.5 V | ALL  | 1, 2, 3              | 3.5<br>7.0<br>11.0    |                      | V     |     |     |
| Low-level input<br>voltage                               | V <sub>IL</sub>   | V <sub>DD</sub> = 5 V, V <sub>O</sub> = 0.5 or 4.5 V<br>V <sub>DD</sub> = 10 V, V <sub>O</sub> = 1.0 or 9.0 V<br>V <sub>DD</sub> = 15 V, V <sub>O</sub> = 1.5 or 13.5 V | ALL  | 1, 2, 3              |                       | 1.5<br>3.0<br>4.0    | V     |     |     |
| Input capacitance  | C <sub>IN</sub>   | V <sub>IN</sub> = 0 V see 4.4.1c  | ALL  | 4                    |                       | 7.5                  | pF    |     |     |
| Quiescent current  | I <sub>DD</sub>   | V <sub>DD</sub> = 5.0 V<br>V <sub>IN</sub> = 0 V or V <sub>DD</sub>   | ALL  | 1, 3<br>2            |                       | 1.0<br>30.0          | μA    |     |     |
|  |                   | V <sub>DD</sub> = 10 V<br>V <sub>IN</sub> = 0 V or V <sub>DD</sub>  | ALL  | 1, 3<br>2            |                       | 2.0<br>60.0          |       |     |     |
|  |                   | V <sub>DD</sub> = 15 V<br>V <sub>IN</sub> = 0 V or V <sub>DD</sub>  | ALL  | 1, 3<br>2            |                       | 4.0<br>120           |       |     |     |
| Input leakage<br>current                                 | I <sub>IN</sub>   | V <sub>IN</sub> = 0 V or 15.0 V   | ALL  | 1, 2, 3              |                       | ±1.0                 | μA    |     |     |
| Functional tests   |                   | See 4.4.1d  | ALL  | 7,8                  |                       |                      |       |     |     |
| Propagation delay,<br>clock to Q or $\bar{Q}$<br>outputs | t <sub>PHL1</sub> | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ  | 01   | 9                    | 1.0                   | 350                  | ns    |     |     |
|  |                   |   | 02   |                      |                       |                      |       | 15  | 400 |
|  |                   |   | 03   |                      |                       |                      |       | 350 |     |
|  | 01                | 10, 11  | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01                   | 1.0                   | 437                  |       |     |     |
|  |                   |   |  | 02                   |                       |                      |       | 23  | 560 |
|  |                   |   |  | 03                   |                       |                      |       | 525 |     |

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TABLE I. Electrical characteristics - Continued.

| Test  | Symbol   | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ 125°C<br>Unless otherwise specified   | Device type       | Group A subgroups  | Limits |     | Units |
|---|--|--|-------------------|--|--------|-----|-------|
|   |  |  |                   |  | Min    | Max |       |
| Propagation delay time low-to-high Level Set to $\bar{Q}$ or Reset to $\bar{Q}$ | t <sub>PLH2</sub>  | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01,02             | 9  | 1.0    | 300 | ns    |
|   |  |  | 03                |  |        | 450 |       |
|   |  | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01                | 10, 11   | 1.0    | 375 |       |
|   |  |  | 02                |  | 23     | 450 |       |
|   |  |  | 03                |  |        | 675 |       |
|   |  | Propagation delay time high-to Low Level Set to $\bar{Q}$ or Reset to Q      | t <sub>PHL2</sub> | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01     | 9   |       |
| 02  | 20   |  |                   |  | 400    |     |       |
| 03  |  |  |                   |  | 450    |     |       |
| V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ    | 01   |  |                   | 10, 11   | 1.0    | 375 |       |
|   | 02   |  |                   |  | 30     | 600 |       |
|   | 03   |  |                   |  |        | 675 |       |
| Transition time   | t <sub>THL'</sub><br>t <sub>TLH</sub>  | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01                | 9  | 1.0    | 200 | ns    |
|   |  |  | 02                |  | 10     | 200 |       |
|   |  |  | 03                |  |        | 200 |       |
|   | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01   | 10, 11            | 1.0  | 300    |     |       |
|   |  | 02   |                   | 15   | 300    |     |       |
|   |  | 03   |                   |  | 300    |     |       |

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TABLE I. Electrical characteristics - Continued.

| Test                         | Symbol           | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ 125°C<br>Unless otherwise specified   | Device<br>type | Group A<br>subgroups | Limits |     | Units |
|------------------------------|------------------|--|----------------|----------------------|--------|-----|-------|
|                              |                  |  |                |                      | Min    | Max |       |
| Maximum clock<br>frequency   | f <sub>MAX</sub> | V <sub>DD</sub> = 5.0<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ   | 01             | 9                    | 3.5    |     | MHz   |
|                              |                  |  | 02             |                      | 2.5    |     |       |
|                              |                  |  | 03             |                      | 2.0    |     |       |
|                              |                  | V <sub>DD</sub> = 5.0 V<br>C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 200 kΩ | 01             | 10, 11               | 2.5    |     |       |
|                              |                  |  | 02             |                      | 2.2    |     |       |
|                              |                  |  | 03             |                      | 1.3    |     |       |
| Minimum clock<br>pulse width | t <sub>CP</sub>  | V <sub>DD</sub> = 5.0 V  | 01,02          | 9                    |        | 200 | ns    |
|                              |                  |  | 03             |                      |        | 250 |       |

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T<sub>A</sub> = 125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-I-38535, appendix A.

|   |                          |                             |                    |
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|                 |                 |
|-----------------|-----------------|
| Device types    | 01, 02, and 03  |
| Case outlines   | C and D         |
| Terminal number | Terminal symbol |
| 1               | Q1              |
| 2               | $\bar{Q}1$      |
| 3               | CLK1            |
| 4               | RESET1          |
| 5               | D1              |
| 6               | SET1            |
| 7               | $V_{SS}$        |
| 8               | SET2            |
| 9               | D2              |
| 10              | RESET2          |
| 11              | CLK2            |
| 12              | Q2              |
| 13              | $\bar{Q}2$      |
| 14              | $V_{DD}$        |

FIGURE 1. Terminal connections.

| Inputs |      |       |     | Outputs |           |
|--------|------|-------|-----|---------|-----------|
| Clock  | Data | Reset | Set | Q       | $\bar{Q}$ |
|        | L    | L     | L   | L       | H         |
|        | H    | L     | L   | H       | L         |
|        | X    | L     | L   | Q       | $\bar{Q}$ |
| X      | X    | H     | L   | L       | H         |
| X      | X    | L     | H   | H       | L         |
| X      | X    | H     | H   | H       | H         |

X = Don't care  
L = Low logic level  
H = High logic level  
 $\bar{Q}$ , Q = No change

FIGURE 2. Truth table.

|  |                    |                              |                     |
|--|--------------------|------------------------------|---------------------|
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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$  measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on five devices with zero failures.
- d. Subgroup 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady state life test conditions, method 1005 of MIL-STD-883. The test circuit shall be maintained by the manufacturer under document revision level control.

(1) Test condition A, B, C, or D.

(2)  $T_A = 125^\circ\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

|  |                                      |
|--|--------------------------------------|
| MIL-STD-883 test requirements  | Subgroups<br>Method 5005,<br>table I |
| Interim electrical parameters<br>(pre burn-in) (method 5004,<br>3.1.8) | ---                                  |
| Final electrical test parameters<br>(method 5004, 3.1.14)              | 1*, 2, 3,<br>9                       |
| Group A test requirements<br>(method 5005)                             | 1, 2, 3, 4, 7,<br>8, 9, 10**11**     |
| Groups C and D end-point<br>electrical parameters<br>(method 5005)     | 1, 2, 3                              |

\* PDA applies to subgroup 1 (see 4.3c).

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, OH 45444-5270 , or telephone 513-296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendor listed in MIL-BUL 103 have agreed to this drawing and a certificate of compliance (see 3.6) has been submitted to and accepted DESC-EC.

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