

# HM53461 Series

65,536-word x 4-bit Multiport CMOS Video RAM

## ■ DESCRIPTION

The HM53461 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

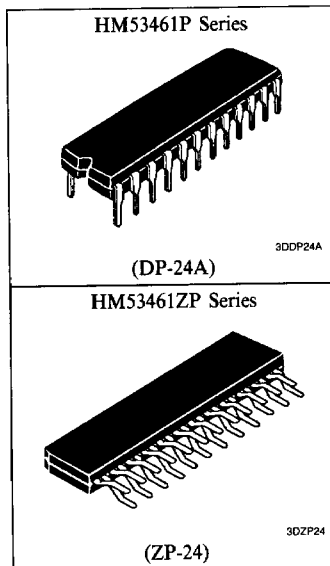
Utilizing the Hitachi 2  $\mu$ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

## ■ FEATURES

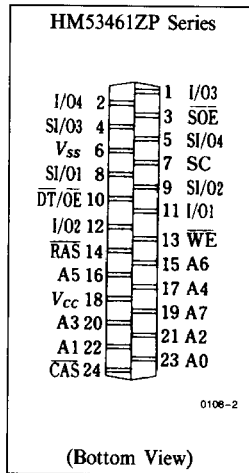
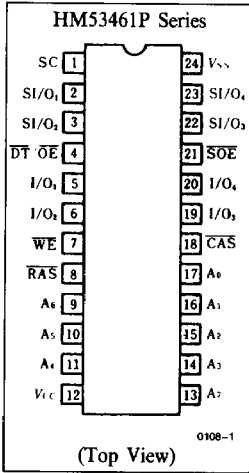
- Multiport Organization  
(RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double Layer Polysilicon/Polyicide n-Well CMOS Process
- Single 5V ( $\pm 10\%$ )
- Low Power
  - Active
    - RAM ..... 380 mW (max)
    - SAM ..... 220 mW (max)
    - Standby ..... 40 mW (max)
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns
  - SAM ..... 40 ns/40 ns/60 ns
- Cycle Time Random Read or Write Cycle Time (RAM) ..... 190 ns/220 ns/260 ns  
Serial Read or Write Cycle Time (SAM) ..... 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles ..... 4 ms
- Refresh Function
  - RAS Only Refresh
  - CAS Before RAS Refresh
  - Hidden Refresh
- Data Transfer Operation (RAM  $\leftrightarrow$  SAM)
- Fast Serial Access Operation Asynchronized with RAM Port Except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability

## ■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53461P-10	100 ns	400 mil 24-pin
HM53461P-12	120 ns	Plastic DIP
HM53461P-15	150 ns	(DP-24A)
HM53461ZP-10	100 ns	24-pin
HM53461ZP-12	120 ns	Plastic ZIP
HM53461ZP-15	150 ns	(ZP-24)



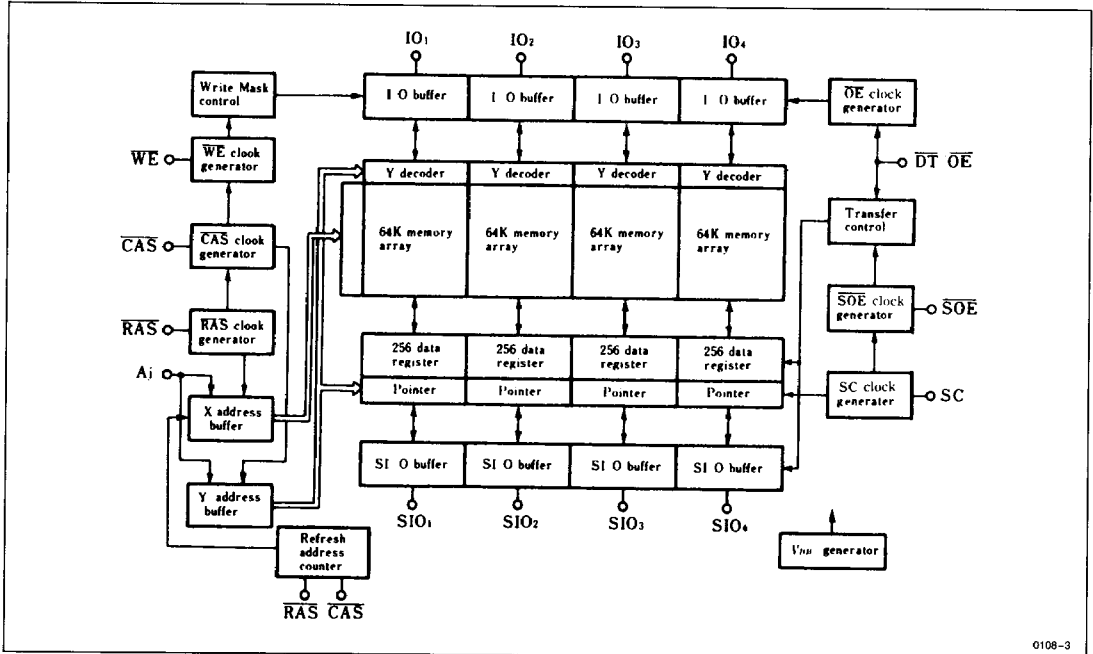
■ PIN OUT



■ PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> -A <sub>7</sub>	Address Inputs
I/O <sub>1</sub> -I/O <sub>4</sub>	RAM Port Data Input/Output
SI/O <sub>1</sub> -SI/O <sub>4</sub>	SAM Port Data Input/Output
RAS	Row Address Strobe
CAS	Column Address Strobe
SC	Serial Clock
WE	Write Enable
DT/OE	Data Transfer/Output Enable
SOE	SAM Port Enable
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	- 1.0 to + 7.0	V
Power Supply Voltage Relative to V <sub>SS</sub>	V <sub>CC</sub>	- 0.5 to + 7.0	V
Operating Temperature, T <sub>A</sub> (Ambient)	T <sub>opr</sub>	0 to + 70	°C
Storage Temperature	T <sub>stg</sub>	- 55 to + 125	°C
Short Circuit Output Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>T</sub>	1.0	W

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T<sub>A</sub> = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V	
Input Low Voltage	V <sub>IL</sub>	- 0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V<sub>SS</sub>.  
 2. - 3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	SAM PORT		HM53461-10	HM53461-12	HM53461-15	Unit	RAM PORT	Note
		Standby	Active					Test Conditions	
Operating Current	I <sub>CC1</sub>	—	×	70	60	50	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling	
	I <sub>CC7</sub>	×	—	110	100	80	mA	t <sub>RC</sub> = Min	
Standby Current	I <sub>CC2</sub>	—	×	7	7	7	mA	$\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$	
	I <sub>CC8</sub>	×	—	40	40	30	mA		
$\overline{\text{RAS}}$ Only Refresh Current	I <sub>CC3</sub>	—	×	60	50	40	mA	CAS = V <sub>IH</sub> , RAS Cycling t <sub>RC</sub> = Min	
	I <sub>CC9</sub>	×	—	100	90	70	mA		
Page Mode Current	I <sub>CC4</sub>	—	×	50	40	35	mA	$\overline{\text{RAS}} = V_{IL}$ , CAS Cycling t <sub>PC</sub> = Min	
	I <sub>CC10</sub>	×	—	90	80	65	mA		
CBR Refresh Current	I <sub>CC5</sub>	—	×	60	50	40	mA	$\overline{\text{RAS}}$ Cycling	
	I <sub>CC11</sub>	×	—	100	90	70	mA	t <sub>RC</sub> = Min	
Data Transfer Current	I <sub>CC6</sub>	—	×	75	65	55	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling t <sub>RC</sub> = Min	
	I <sub>CC12</sub>	×	—	115	105	85	mA		

Parameter	Symbol	Min	Max	Unit	Test Conditions	Note
Input Leakage	I <sub>LI</sub>	- 10	10	μA		
Output Leakage	I <sub>LO</sub>	- 10	10	μA		
Output High Voltage	V <sub>OH</sub>	2.4	—	V	I <sub>OH</sub> = - 2 mA	
Output Low Voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 4.2 mA	

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C <sub>I1</sub>	—	5	pF	
Clocks	C <sub>I2</sub>	—	5	pF	
I/O, SI/O	C <sub>I/O</sub>	—	7	pF	



■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(T<sub>A</sub> = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)<sup>1, 10, 11</sup>

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t <sub>RC</sub>	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t <sub>RWC</sub>	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t <sub>PC</sub>	70	—	85	—	105	—	ns	
Access Time from RAS	t <sub>RAC</sub>	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t <sub>CAC</sub>	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn-off Delay Referenced to CAS	t <sub>OFF1</sub>	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	6
RAS Precharge Time	t <sub>RP</sub>	80	—	90	—	100	—	ns	
RAS Pulse Width	t <sub>RAS</sub>	100	10000	120	10000	150	10000	ns	
CAS Pulse Width	t <sub>CAS</sub>	50	10000	60	10000	75	10000	ns	
RAS to CAS Delay Time	t <sub>RCSD</sub>	25	50	25	60	30	75	ns	7
RAS Hold Time	t <sub>RSH</sub>	50	—	60	—	75	—	ns	
CAS Hold Time	t <sub>CSH</sub>	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t <sub>CRP</sub>	10	—	10	—	10	—	ns	
Row Address Setup Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	15	—	15	—	20	—	ns	
Column Address Setup Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	20	—	20	—	25	—	ns	
Write Command Setup Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	8
Write Command Hold Time	t <sub>WCH</sub>	25	—	25	—	30	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	15	—	20	—	25	—	ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	35	—	40	—	45	—	ns	
Write Command to CAS Lead Time	t <sub>CWL</sub>	35	—	40	—	45	—	ns	
Data-in Setup Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	9
Data-in Hold Time	t <sub>DH</sub>	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to RAS	t <sub>RRH</sub>	10	—	10	—	10	—	ns	
Refresh Period	t <sub>REF</sub>	—	4	—	4	—	4	ms	
RAS Pulse Width (Read-Modify-Write Cycle)	t <sub>RWS</sub>	170	10000	200	10000	245	10000	ns	
CAS to WE Delay	t <sub>CWD</sub>	85	—	100	—	125	—	ns	8
CAS Setup Time (CAS Before RAS Refresh)	t <sub>CSR</sub>	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh)	t <sub>CHR</sub>	20	—	25	—	30	—	ns	
RAS Precharge to CAS Hold Time	t <sub>RPC</sub>	10	—	10	—	10	—	ns	
CAS Precharge Time	t <sub>CP</sub>	10	—	15	—	20	—	ns	
Access Time from OE	t <sub>OAC</sub>	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay referenced to OE	t <sub>OFF2</sub>	0	25	0	30	0	40	ns	
OE to Data-in Delay Time	t <sub>ODD</sub>	25	—	30	—	40	—	ns	
OE Hold Time referenced to WE	t <sub>OEH</sub>	10	—	15	—	20	—	ns	
Data-in to CAS Delay Time	t <sub>DZC</sub>	0	—	0	—	0	—	ns	
Data-in to OE Delay Time	t <sub>DZO</sub>	0	—	0	—	0	—	ns	
OE to RAS Delay Time	t <sub>ORD</sub>	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t <sub>SCC</sub>	40	—	40	—	60	—	ns	
Access Time from SC	t <sub>SCA</sub>	—	40	—	40	—	60	ns	10
Access Time from SOE	t <sub>SEA</sub>	—	25	—	30	—	40	ns	10



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ )<sup>1, 10, 11</sup> (continued)

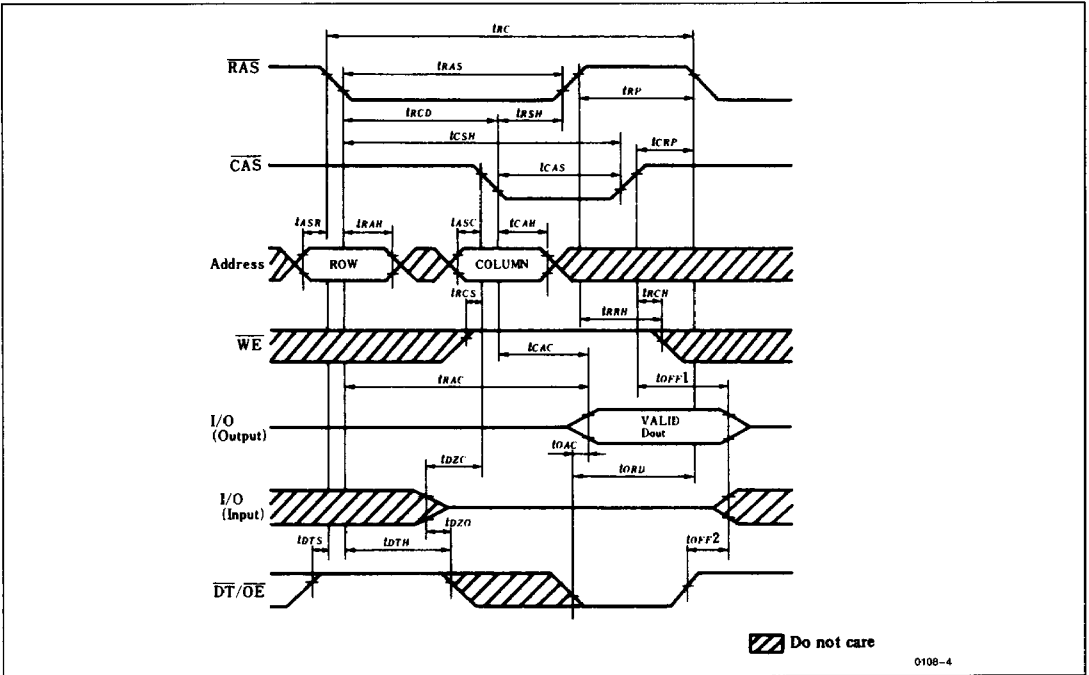
Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
SC Pulse Width	$t_{SC}$	10	—	10	—	10	—	ns	
SC Precharge Width	$t_{SCP}$	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	$t_{SOH}$	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	$t_{SEZ}$	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	$t_{SIS}$	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	$t_{SIH}$	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	$t_{DTS}$	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	$t_{RDH}$	80	—	90	—	110	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	$t_{DTH}$	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	$t_{CDH}$	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	$t_{SDD}$	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	$t_{SDH}$	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	$t_{DTR}$	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	$t_{WS}$	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	$t_{WH}$	15	—	15	—	20	—	ms	
I/O to $\overline{RAS}$ Setup Time	$t_{MS}$	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ Hold Time	$t_{MH}$	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	$t_{SRZ}$	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	$t_{SRS}$	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC Delay Time	$t_{SRD}$	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	$t_{SID}$	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{DT}$ Delay Time	$t_{SZD}$	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	$t_{ES}$	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	$t_{EH}$	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	$t_{SWS}$	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	$t_{SWH}$	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	$t_{SWIS}$	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	$t_{SWIH}$	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	$t_{DLZ}$	5	—	10	—	10	—	ns	

- Notes:
- AC measurements assume  $t_T = 5$  ns.
  - Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  - Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  - Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
  - $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  - $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  - Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  - $t_{WCS}$  and  $t_{CWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \geq t_{CWD}(\text{min})$ , the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  - These parameters are referenced to  $\overline{CAS}$  leading edge in an early write cycle and to  $\overline{WE}$  leading edge in a delayed write or a read-modify-write cycle.
  - Measured with a load circuit equivalent to 2 TTL and 50 pF.
  - An initial pause of 100  $\mu\text{s}$  is required after power-up. Then execute at least 8 initialization cycles.

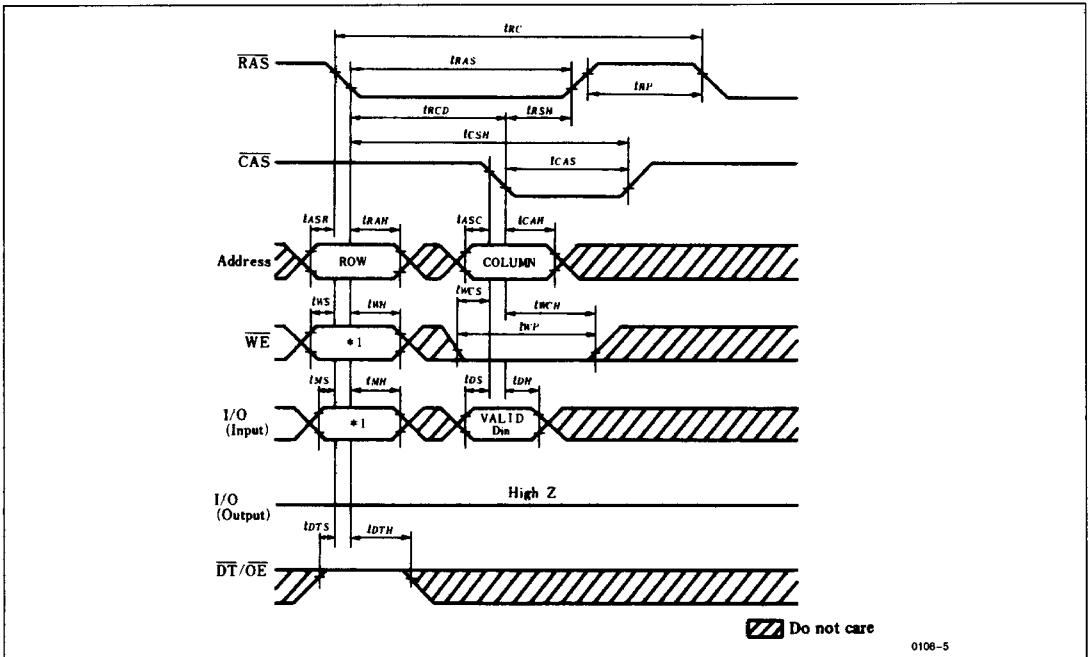


■ TIMING WAVEFORMS

• Read Cycle



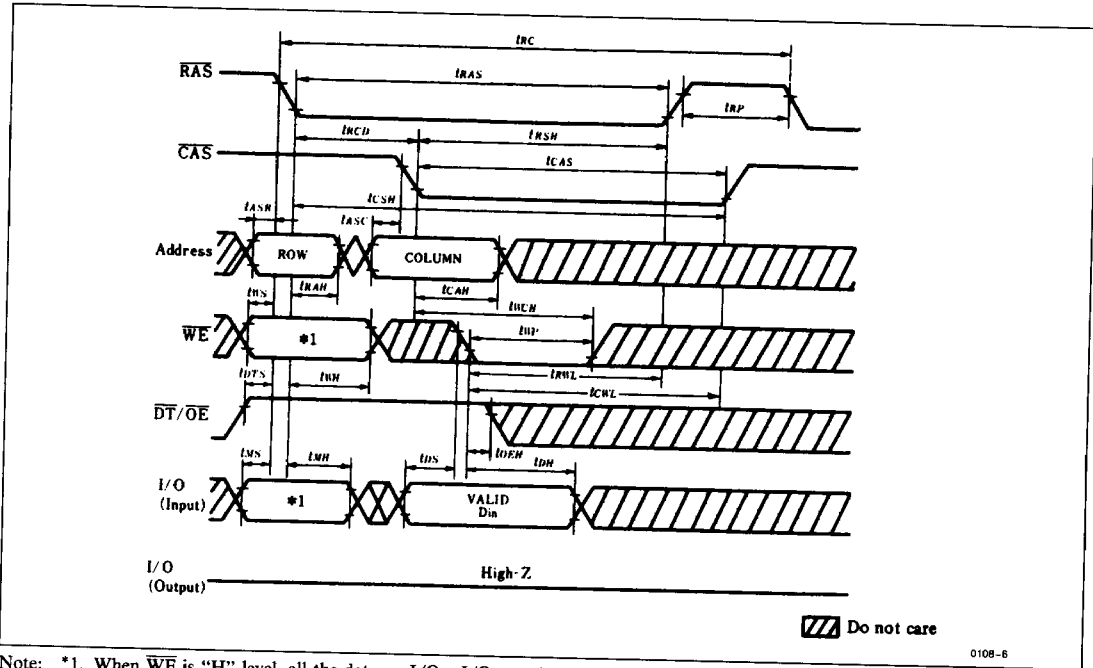
• Early Write Cycle



Note: \*1. When  $\overline{WE}$  is "H" level, all the data on the I/O can be written into the cell.  
When  $\overline{WE}$  is "L" level, the data on the I/O are not written except for when I/O is "high" at the falling edge of  $\overline{RAS}$ .

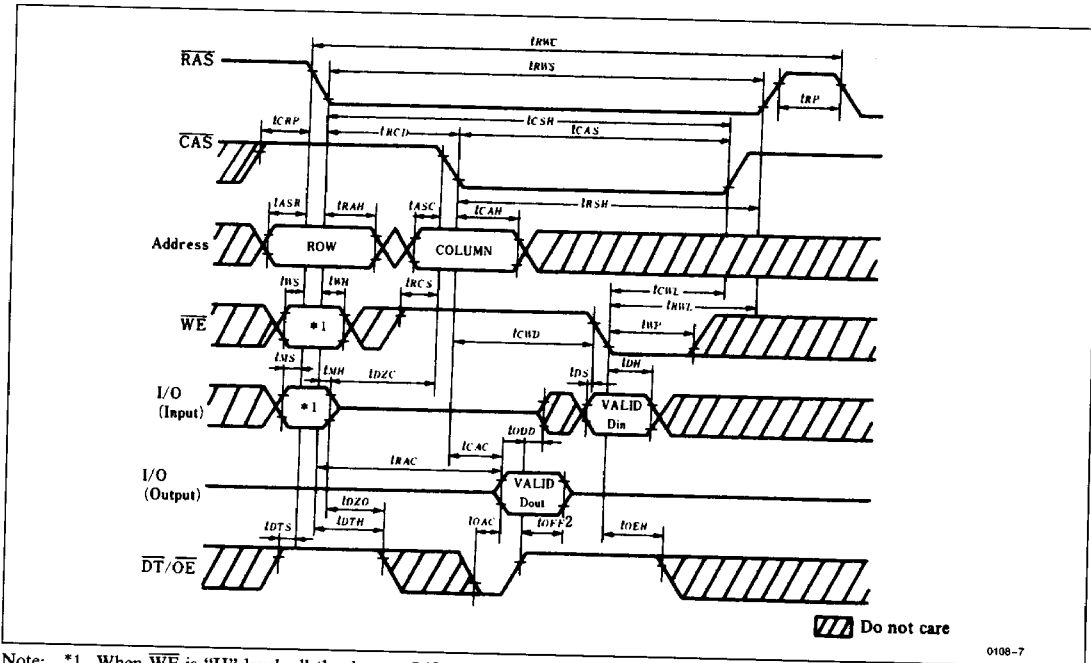


**• Delayed Write Cycle**



Note: \*1. When  $\overline{WE}$  is "H" level, all the data on  $I/O_1-I/O_4$  can be written into the memory cell.  
When  $\overline{WE}$  is "L" level, the data on I/Os are not written except for when  $I/O = "H"$  at the falling edge of  $\overline{RAS}$ .

**• Read-Modify-Write Cycle**

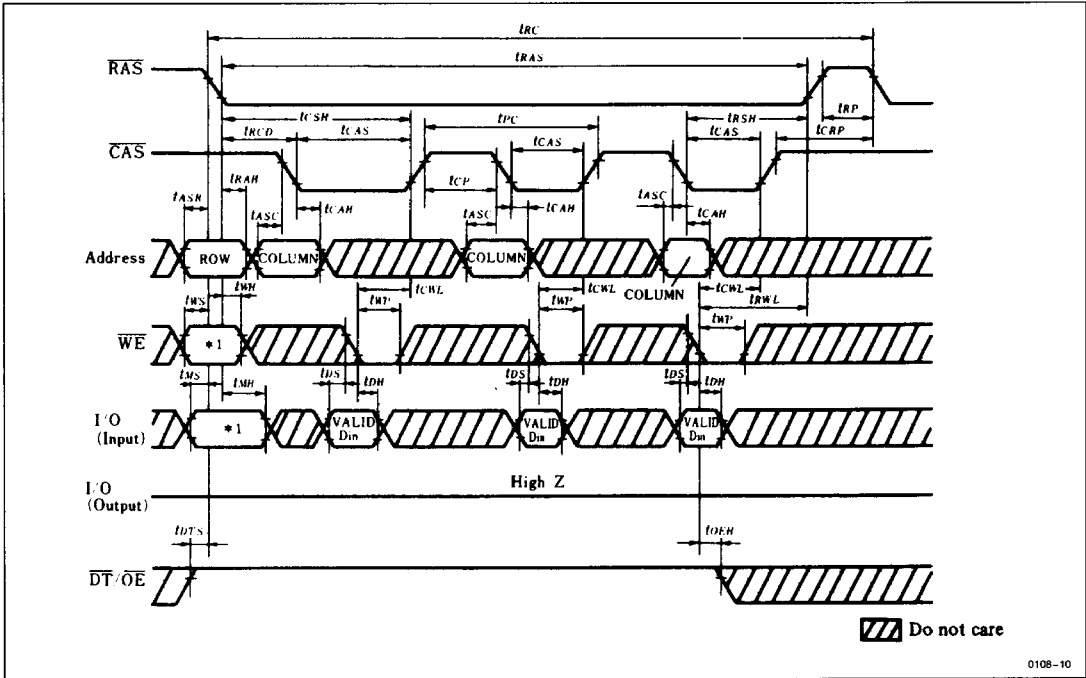


Note: \*1. When  $\overline{WE}$  is "H" level, all the data on  $I/O_1-I/O_4$  can be written into the memory cell.  
When  $\overline{WE}$  is "L" level, the data on I/Os are not written except for when  $I/O = "H"$  at the falling edge of  $\overline{RAS}$ .



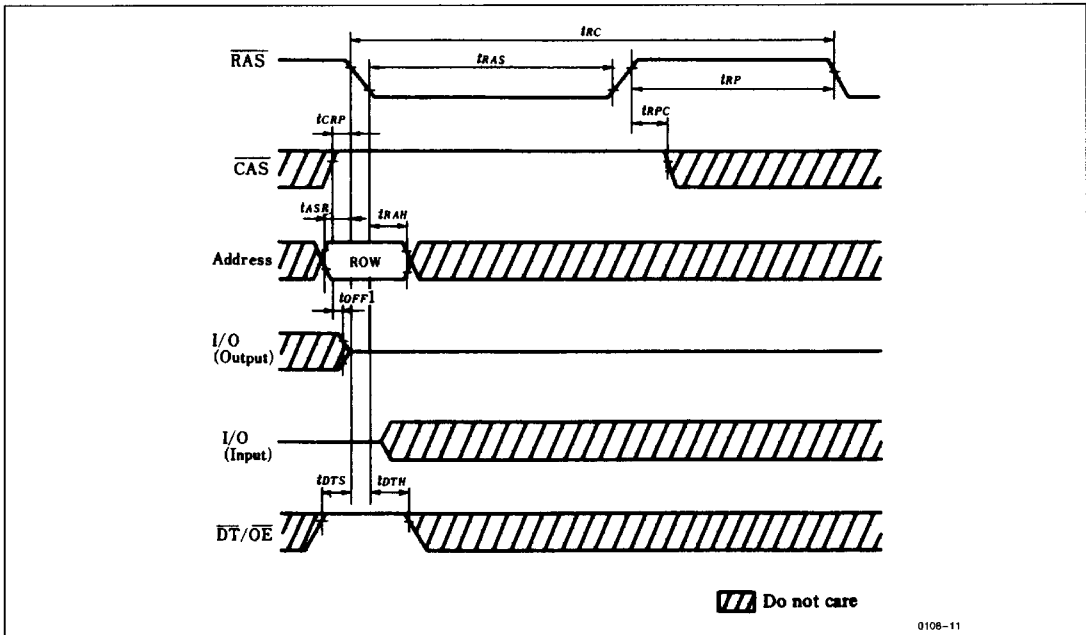


• Page Mode Write Cycle (Delayed Write)

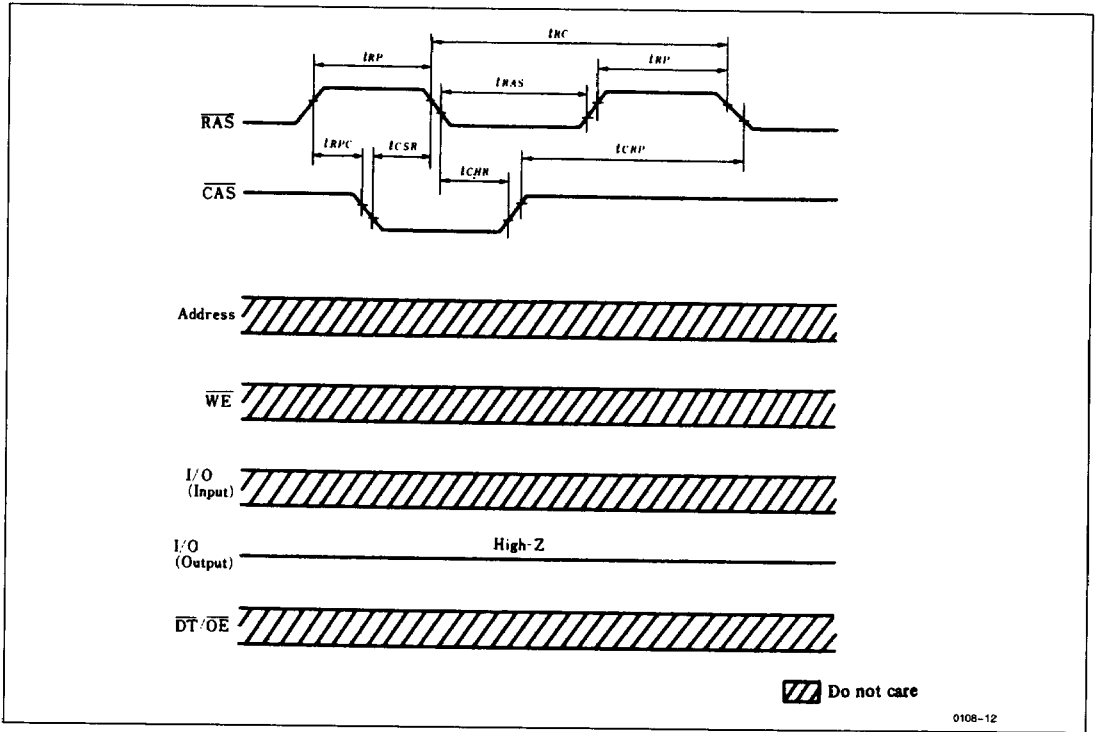


Note: \*1. When  $\overline{WE}$  is "H" level, all the data on I/O<sub>1</sub>-I/O<sub>4</sub> can be written into the memory cell.  
 When  $\overline{WE}$  is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of  $\overline{RAS}$ .

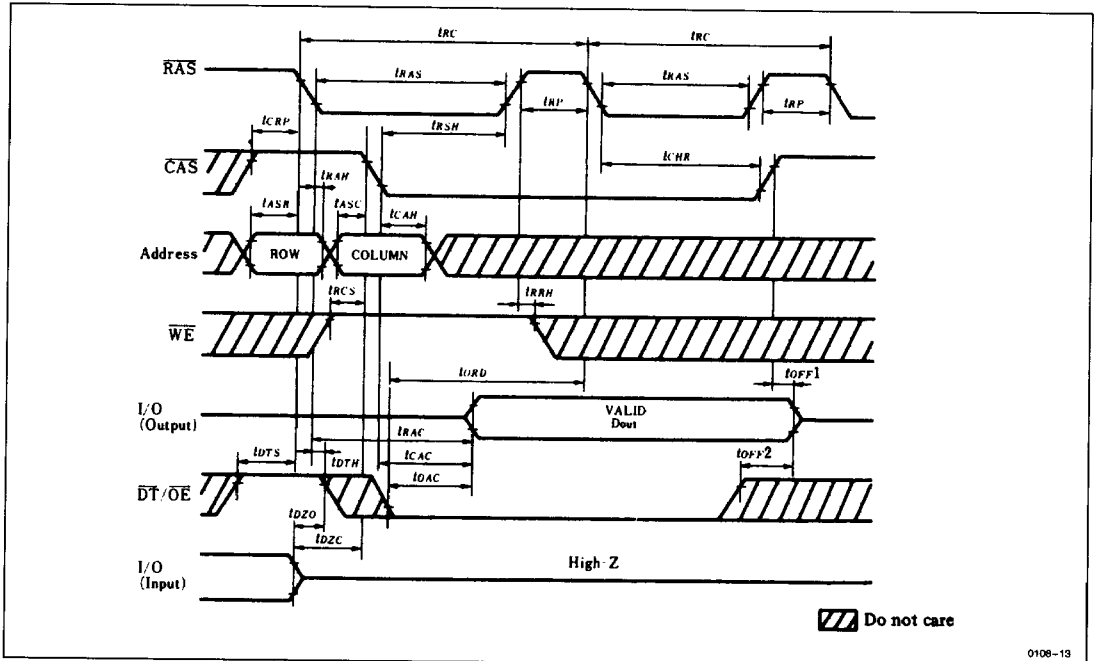
•  $\overline{RAS}$  Only Refresh Cycle



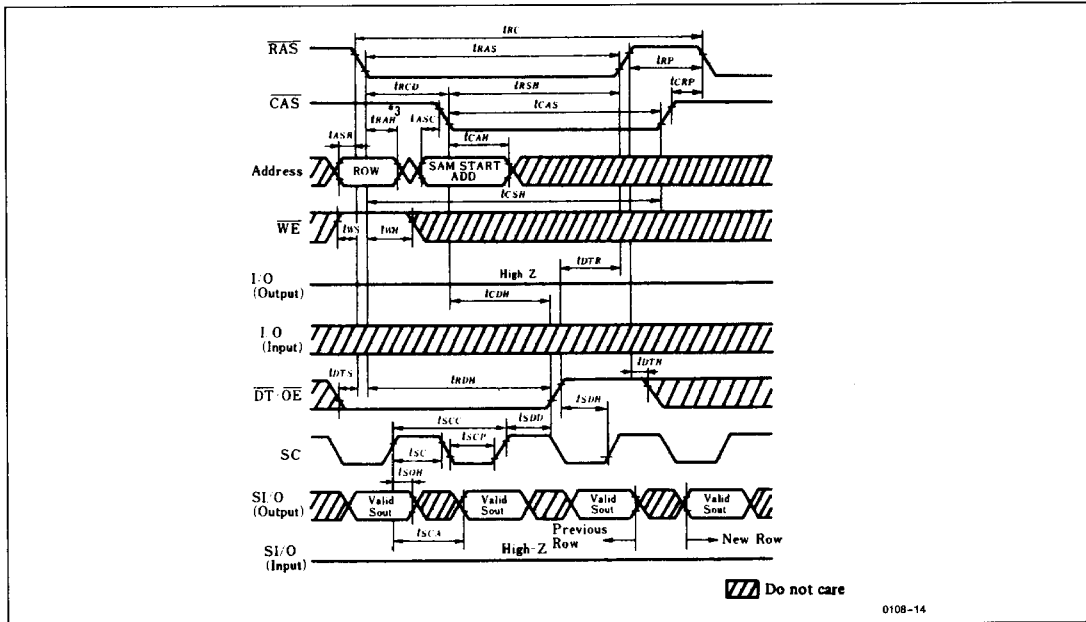
• CAS Before RAS Refresh Cycle



• Hidden Refresh Cycle

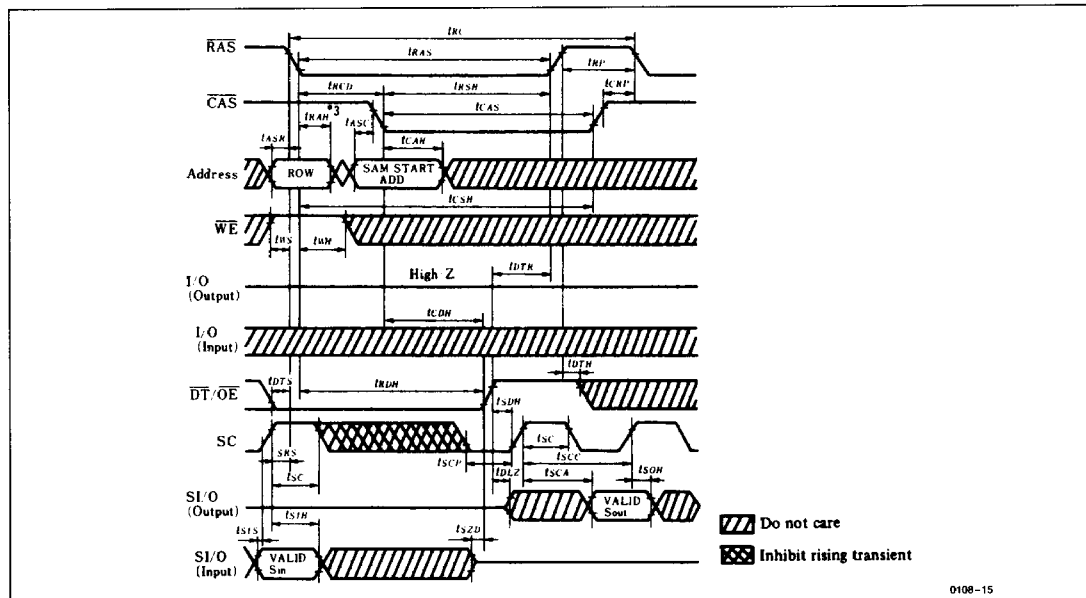


• Read Transfer Cycle (1)\*1, \*2



- Notes:
- \*1. In the case that the previous data transfer cycle was read transfer.
  - \*2. Assume that SOE is "L" level.
  - \*3. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

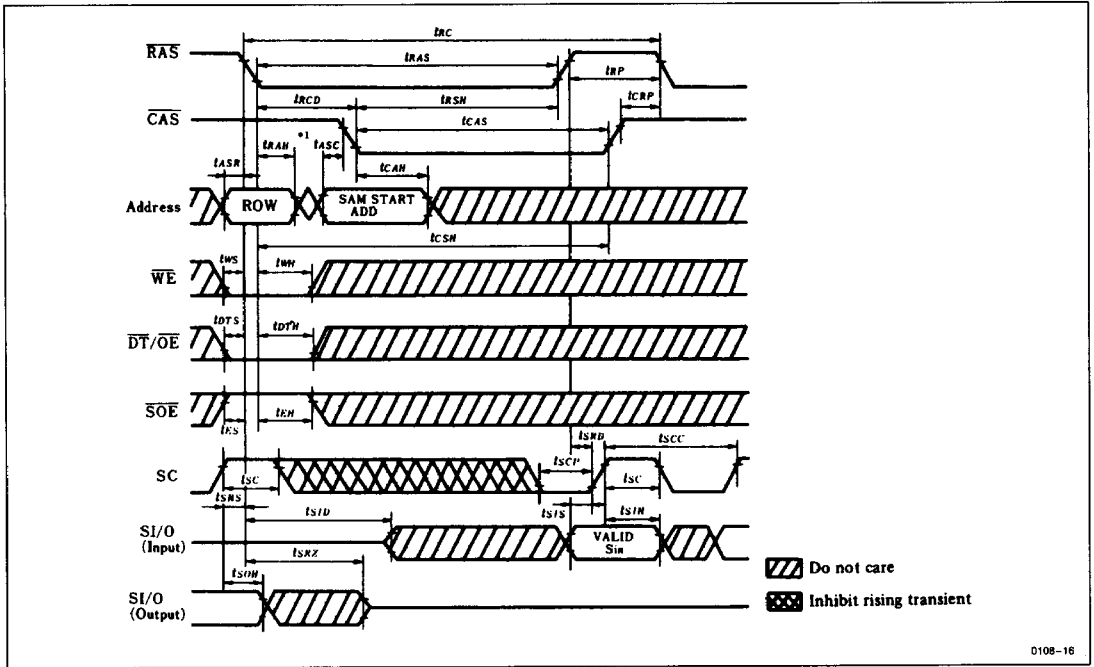
• Read Transfer Cycle (2)\*1, \*2



- Notes:
- \*1. In the case that the previous data transfer cycle was write transfer or pseudo transfer.
  - \*2. Assume that SOE is "L" level.
  - \*3. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

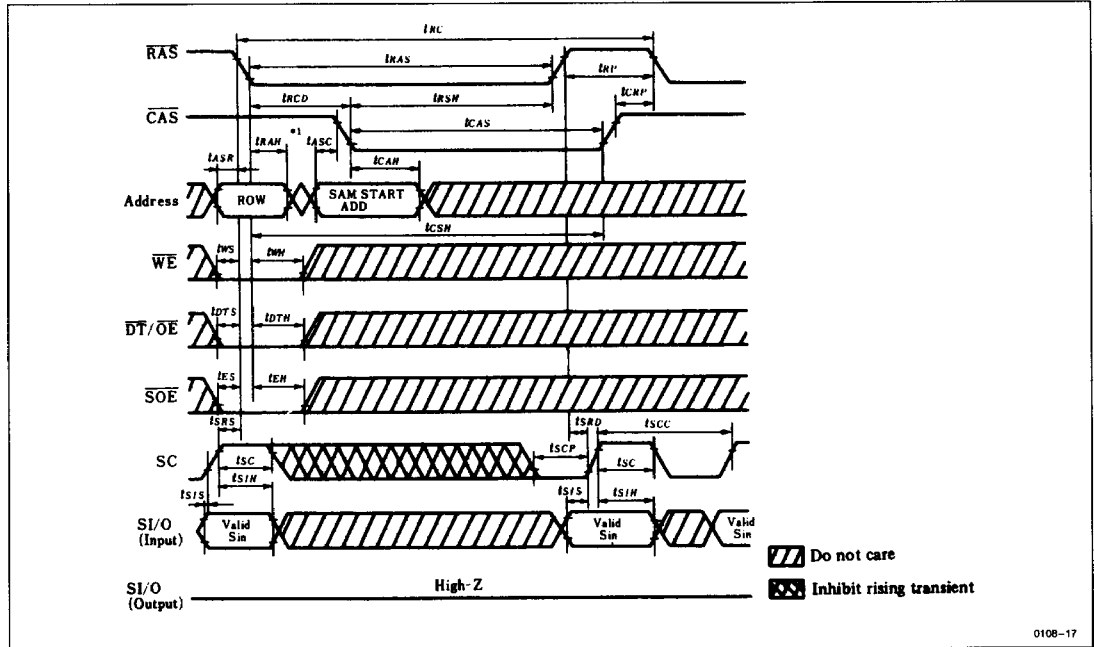


• Pseudo Transfer Cycle



Note: \*1. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

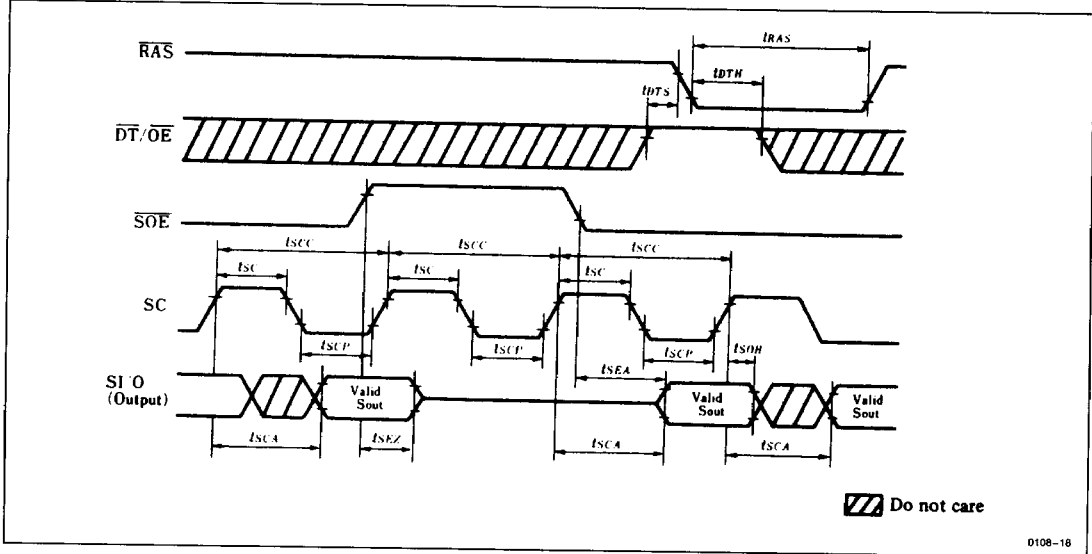
• Write Transfer Cycle



Note: \*1. CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.



• Serial Read Cycle



• Serial Write Cycle

