



N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			Die [†]
60V	3.0W	2.0A	VN01506NW
90V	3.0W	2.0A	VN1509NW

[†] MIL visual screening available.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

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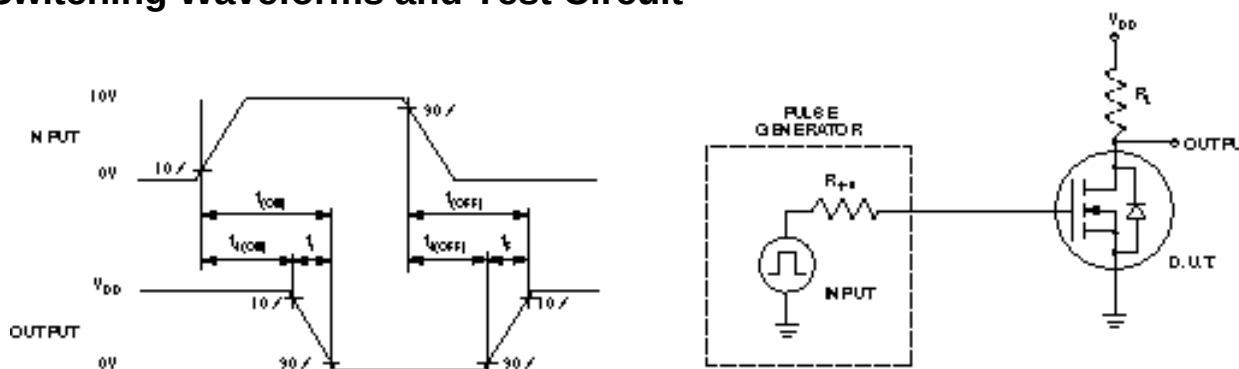
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	VN1509	90			V	V _{GS} = 0V, I _D = 1mA
		VN1506	60				
V _{GS(th)}	Gate Threshold Voltage		0.8		2.4	V	V _{GS} = V _{DS} , I _D = 1mA
DV _{GS(th)}	Change in V _{GS(th)} with Temperature			-3.8	-5.5	mV/°C	V _{GS} = V _{DS} , I _D = 1mA
I _{GSS}	Gate Body Leakage				100	nA	V _{GS} = ± 20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current				1	μA	V _{GS} = 0V, V _{DS} = Max Rating
					100		V _{GS} = 0V, V _{DS} = 0.8 Max Rating T _A = 125°C
I _{D(ON)}	ON-State Drain Current		0.5	1.0		A	V _{GS} = 5V, V _{DS} = 25V
			2.0	2.5			V _{GS} = 10V, V _{DS} = 25V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance			3.0	5.0	W	V _{GS} = 5V, I _D = 250mA
				2.5	3.0		V _{GS} = 10V, I _D = 1A
DR _{DS(ON)}	Change in R _{DS(ON)} with Temperature			0.70	1	%/°C	V _{GS} = 10V, I _D = 1A
G _{FS}	Forward Transconductance		300	450		mS	V _{DS} = 25V, I _D = 0.5A
C _{ISS}	Input Capacitance			55	65	pF	V _{GS} = 0V, V _{DS} = 25V f = 1 MHz
C _{OSS}	Common Source Output Capacitance			20	25		
C _{RSS}	Reverse Transfer Capacitance			5	8		
t _{d(ON)}	Turn-ON Delay Time			3	5	ns	V _{DD} = 25V I _D = 1A R _{GEN} = 25W
t _r	Rise Time			5	8		
t _{d(OFF)}	Turn-OFF Delay Time			6	9		
t _f	Fall Time			5	8		
V _{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V _{GS} = 0V, I _{SD} = 1.0A
t _{rr}	Reverse Recovery Time			400		ns	V _{GS} = 0V, I _{SD} = 1.0A

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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