

P54/74FCT191T/AT/CT UP-DOWN BINARY COUNTERS

FEATURES

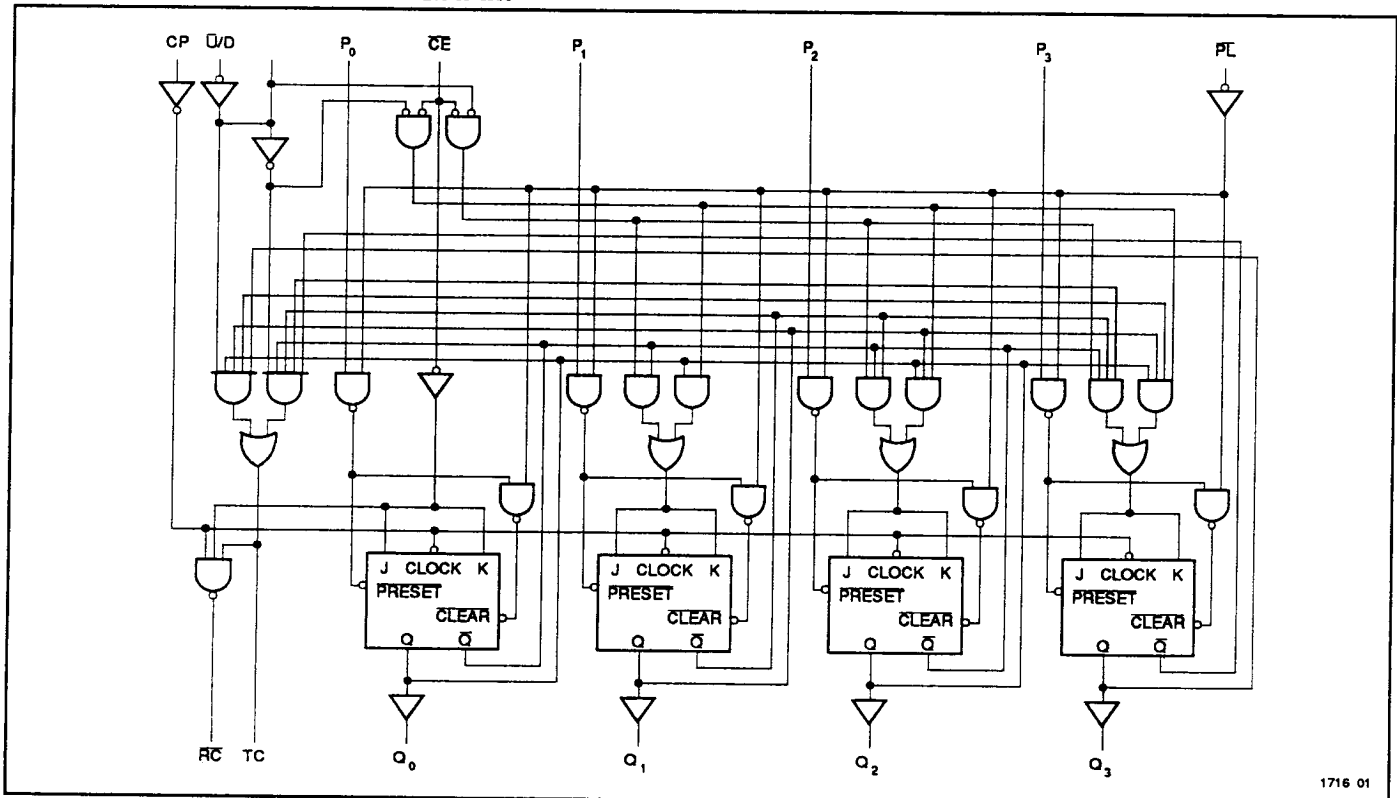
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 6.2ns max. (Com'I)**
FCT-A speed at 7.8ns max. (Com'I)
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'I), 32 mA (MII)**
15 mA Source Current (Com'I), 12 mA (MII)
- **3-State Outputs**
- **Manufactured in 0.7 micron PACE Technology™**

★ DESCRIPTION

The 'FCT191T are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting. The preset allows the 'FCT191T to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The 'FCT191T are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

★ FUNCTIONAL BLOCK DIAGRAM



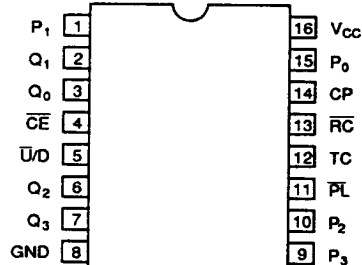
PERFORMANCE
SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

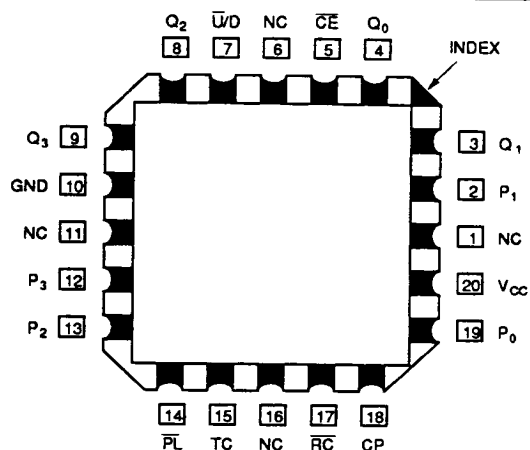
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PIN CONFIGURATIONS



DIP (P10, D10)
SOIC (S10)



LCC (L2)

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DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U/D}$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
RC	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

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RC FUNCTION TABLE⁽²⁾

Inputs		Outputs	
$\overline{CE}$	CP	TC ⁽¹⁾	$\overline{RC}$
L		H	
H	X	X	H
X	X	L	H

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MODE SELECT FUNCTION TABLE⁽²⁾

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

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Notes:

1. TC is generated internally.

2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care,  = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	-0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

Notes:

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1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	-0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	-0.5 to +7.0	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		
V _{IL}	Input LOW Voltage				0.8	V		
V _H	Hysteresis			0.2		V		All inputs
V _{IK}	Input Clamp Diode Voltage			−0.7	−1.2	V	MIN	I _{IN} = −18mA
V _{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I _{OH} = −12mA
		Commercial	2.4	3.3		V	MIN	I _{OH} = −15mA
V _{OL}	Output LOW Voltage	Military Commercial Commercial		0.3	0.5	V	MIN	I _{OL} = 32mA
				0.3	0.5	V	MIN	I _{OL} = 48mA
				0.3	0.5	V	MIN	I _{OL} = 64mA
I _I	Input HIGH Current				20	μA	MAX	V _{IN} = V _{CC}
I _{IH}	Input HIGH Current				5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current				−5	μA	MAX	V _{IN} = 0.5V
I _{OS}	Output Short Circuit Current ²		−60	−120	−225	mA	MAX	V _{OUT} = 0.0V
I _{OFF}	Power-off Disable				100	μA	0V	V _{OUT} = 4.5V
C _{IN}	Input Capacitance ³			5	10	pF	MAX	All inputs
C _{OUT}	Output Capacitance ³			9	12	pF	MAX	All outputs
I _{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} − 0.2V

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Notes:

1. Typical limits are at $V_{CC} = 5.0V$, $T_A = +25^\circ C$ ambient.
 2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

- operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
 3. This parameter is guaranteed but not tested.



DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions ⁶
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	0.5	2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f_1 = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, $\overline{MR} = V_{CC} = \overline{SR}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	1.0	2.8	mA	$V_{CC} = \text{MAX}$, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} = V_{CC}$, $V_{IN} = \text{GND}$
		1.2	3.8	mA	$V_{CC} = \text{MAX}$, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} = 3.4V$, $V_{IN} = \text{GND}$
		3.2	6.5 ⁴	mA	$V_{CC} = \text{MAX}$, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 5\text{MHz}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} = V_{CC}$, $V_{IN} = \text{GND}$,
		4.2	10.5 ⁴	mA	$V_{CC} = \text{MAX}$, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 5\text{MHz}$, $\overline{PL} = \overline{CE} = \overline{U/D} = CP = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_i)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_1 = Input Frequency

N_i = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Condition ¹	'FCT191T				'FCT191AT				'FCT191CT				Units
			MIL		COM'L		MIL		COM'L		MIL		COM'L		
			Min. ²	Max.	Min. ²	Max.	Min. ²	Max.	Min. ²	Max.	Min. ²	Max.	Min. ²	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	$C_L = 50pF$ $R_L = 500\Omega$	1.5	16.0	2.5	12.0	1.5	10.5	2.5	7.8	1.5	8.4	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		2.0	16.0	3.0	14.0	2.0	12.2	3.0	11.8	1.5	9.8	1.5	9.4	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		1.5	12.5	2.5	8.5	1.5	10.0	2.5	8.5	1.5	7.9	1.5	6.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.5	2.0	8.0	2.0	8.0	2.0	7.2	1.5	6.4	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U/D}$ to $\overline{RC}$		4.0	22.5	4.0	20.0	4.0	14.7	4.0	13.0	2.5	11.7	2.5	11.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U/D}$ to TC		3.0	13.0	3.0	11.0	3.0	8.5	3.0	7.2	1.5	6.8	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		1.5	16.0	2.0	14.0	1.5	10.4	2.0	9.1	1.5	8.3	1.5	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	14.0	3.0	13.0	3.0	9.1	3.0	8.5	2.0	7.3	2.0	7.2	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		6.0		5.0		5.0		4.0		4.0		3.5		
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5		1.5		1.5		1.5		1.5		1.0		ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.5		10.0		9.5		9.0		7.6		7.2		ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0		0		0		0		0		0		ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U/D}$ to CP		12.0		12.0		10.0		10.0		8.5		8.0		ns
t_H	Hold Time, HIGH or LOW $\overline{U/D}$ to CP		0		0		0		0		0		0		ns
t_W	$\overline{PL}$ Pulse Width LOW	8.5		6.0		8.0		5.5		6.0		5.0		ns	
t_W	Clock Pulse Width HIGH or LOW	7.0		5.0		6.0		4.0 ³		5.0		4.0 ³		ns	
t_{REM}	Recovery Time $\overline{PL}$ to CP	7.5		6.0		6.5		5.0		5.0		4.5		ns	

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

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ORDERING INFORMATION

<u>PxxFCT</u> Temp. Class	<u>xxxx</u> Device type	<u>x</u> Package	<u>x</u> Processing	
				Blank Commercial
				M Military Temperature
				B MIL-STD-883, Class B
				P Plastic DIP
				D CERDIP
				SO Small Outline IC
				L Leadless Chip Carrier
				191T Up/Down Binary Counter
				191AT Fast Up/Down Binary Counter
				191CT Ultra Fast Up/Down Binary Counter
				74 Commercial
				54 Military

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