# P54/74FCT157T/AT/CT
# P54/74FCT158T/AT/CT
# DATA SELECTOR/MULTIPLEXER

## FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.3ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced $V_{OH}$ (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Manufactured in 0.7 micron PACE Technology™**

## DESCRIPTION

The 'FCT157T and 'FCT158T are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data Select input (S). The Enable input ($\overline{E}$) is active-low. When $\overline{E}$ is HIGH, all of the inputs (Y) are forced LOW regardless of all other input conditions.

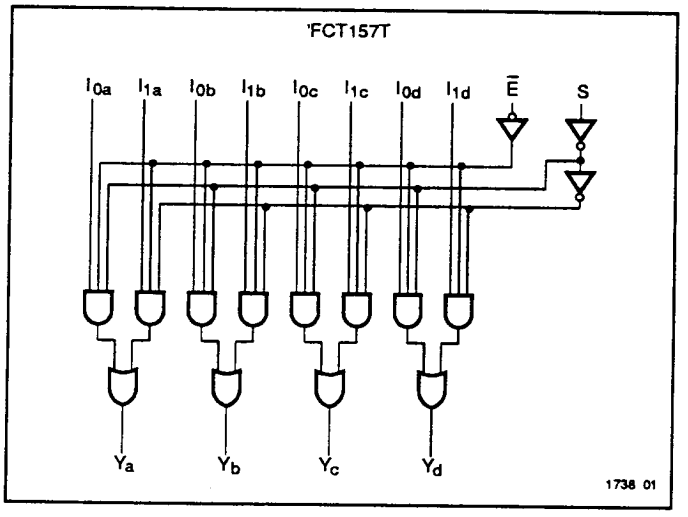
Moving data from two groups of registers to four common output busses is a common use of the 'FCT157T and 'FCT158T. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

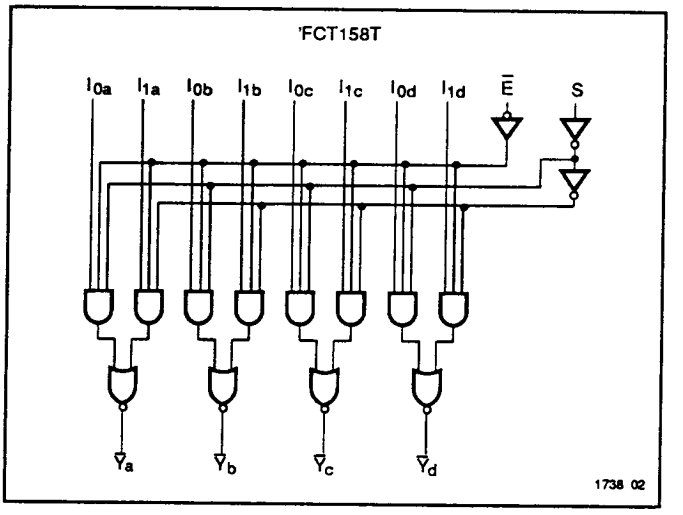
These devices are logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input. The outputs of the 'FCT157T are Non-Inverting whereas the 'FCT158T has Inverting outputs.

The 'FCT157T/158T is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. Pace Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 enviroment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

## FUNCTIONAL BLOCK DIAGRAM

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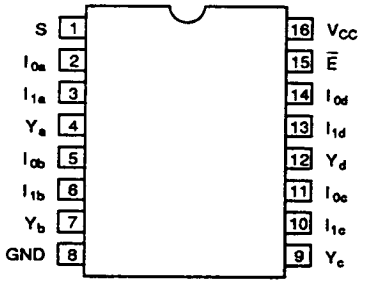
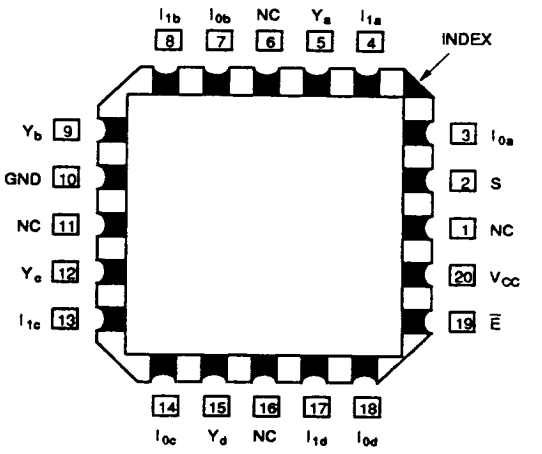
2/13/92 - 8

## PIN CONFIGURATIONS

'FCT157T




DIP (P10, D10)
SOIC (S10)

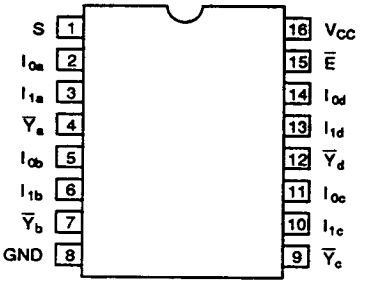



LCC (L2)

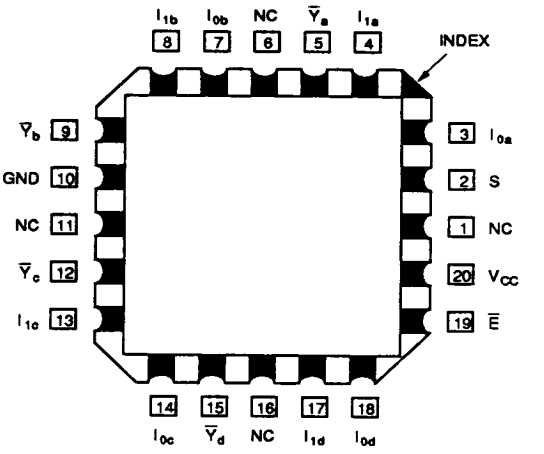
1738 03

## PIN CONFIGURATIONS

'FCT158T




DIP (P10, D10)
SOIC (S10)

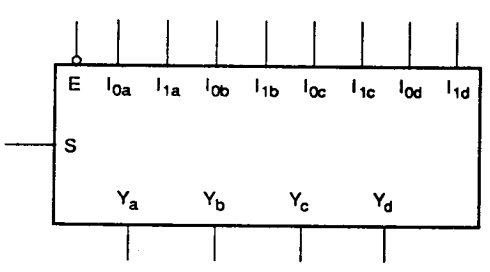



LCC (L2)

1738 04

## LOGIC SYMBOL

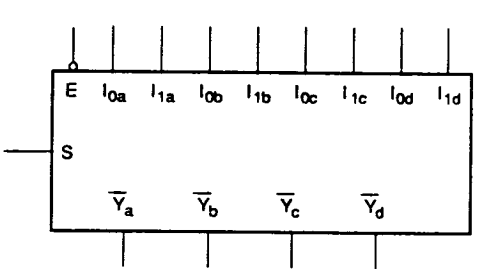
'FCT157T




1738 05

## LOGIC SYMBOL

'FCT158T




1738 06

## ABSOLUTE MAXIMUM RATINGS[1,2]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_A$ | Ambient Temperature Under Bias | –65 to +135 | °C |
| $V_{CC}$ | $V_{CC}$ Potential to Ground | –0.5 to +7.0 | V |
| $P_T$ | Power Dissipation | 0.5 | W |

1738 Tbl 01

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{OUTPUT}$ | Current Applied to Output | 120 | mA |
| $V_{IN}$ | Input Voltage | –0.5 to +7.0 | V |
| $V_{OUT}$ | Voltage Applied to Output | –0.5 to +7.0 | V |

1738 Tbl 02

**Notes:**

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.

## RECOMMENDED OPERATING CONDITIONS

| Free Air Ambient Temperature | Min | Max |
|---|---|---|
| Military | –55°C | +125°C |
| Commercial | 0°C | +70°C |

1738 Tbl 03

| Supply Voltage ($V_{CC}$) | Min | Max |
|---|---|---|
| Military | +4.5V | +5.5V |
| Commercial | +4.75V | +5.25V |

1738 Tbl 04

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Symbol | Parameter | | Min | Typ[1] | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | |
| $V_H$ | Hysteresis | | | 0.2 | | V | | All inputs |
| $V_{IK}$ | Input Clamp Diode Voltage | | | –0.7 | –1.2 | V | MIN | $I_{IN}$ = –18mA |
| $V_{OH}$ | Output HIGH Voltage | Military | 2.4 | 3.3 | | V | MIN | $I_{OH}$ = –12mA |
| | | Commercial | 2.4 | 3.3 | | V | MIN | $I_{OH}$ = –15mA |
| $V_{OL}$ | Output LOW Voltage | Military | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 32mA |
| | | Commercial | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 48mA |
| | | Commercial | | 0.3 | 0.5 | V | MIN | $I_{OL}$ = 64mA |
| $I_I$ | Input HIGH Current | | | | 20 | µA | MAX | $V_{IN}$ = $V_{CC}$ |
| $I_{IH}$ | Input HIGH Current | | | | 5 | µA | MAX | $V_{IN}$ = 2.7V |
| $I_{IL}$ | Input LOW Current | | | | –5 | µA | MAX | $V_{IN}$ = 0.5V |
| $I_{OZH}$ | Off State $I_{OUT}$ HIGH-Level Output Current | | | | 10 | µA | MAX | $V_{OUT}$ = 2.7V |
| $I_{OZL}$ | Off State $I_{OUT}$ LOW-Level Output Current | | | | –10 | µA | MAX | $V_{OUT}$ = 0.5V |
| $I_{OS}$ | Output Short Circuit Current[2] | | –60 | –120 | –225 | mA | MAX | $V_{OUT}$ = 0.0V |
| $I_{OFF}$ | Power-off Disable | | | | 100 | µA | 0V | $V_{OUT}$ = 4.5V |
| $C_{IN}$ | Input Capacitance[3] | | | 5 | 10 | pF | MAX | All inputs |
| $C_{OUT}$ | Output Capacitance[3] | | | 9 | 12 | pF | MAX | All outputs |
| $I_{CC}$ | Quiescent Power Supply Current | | | 0.2 | 1.5 | mA | MAX | $V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ |

1738 Tbl 05

**Notes:**

1. Typical limits are at $V_{CC}$ = 5.0V, $T_A$ = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{os}$ tests should be performed last.
3. This parameter is guaranteed but not tested.

## DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Typ.[1] | Max. | Units | Conditions |
|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs) | 0.5 | 2.0 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 3.4V[2], $f_1$ = 0, Outputs Open |
| $I_{CCD}$ | Dynamic Power Supply Current[3] | 0.15 | 0.25 | mA/ mHz | $V_{CC}$ = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$ |
| $I_C$ | Total Power Supply Current[5] | 1.7 | 4.0 | mA | $V_{CC}$ = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1$ = 10MHz, $\overline{OE}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$ |
| | | 2.0 | 5.0 | mA | $V_{CC}$ = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at $f_1$ = 10MHz, $\overline{OE}$ = GND, $V_{IN}$ = 3.4V or $V_{IN}$ = GND |
| | | 1.7 | 4.0[4] | mA | $V_{CC}$ = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$ = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$ |
| | | 2.7 | 8.0[4] | mA | $V_{CC}$ = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$ = 2.5MHz, $\overline{OE}$ = GND, $V_{IN}$ = 3.4V or $V_{IN}$ = GND |

1738 Tbl 06

**Notes:**

1. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   $I_{CC}$ = Quiescent Current with CMOS input levels
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_0$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_1$ = Input Frequency
   $N_1$ = Number of Inputs at $f_1$
   All currents are in milliamps and all frequencies are in megahertz.

## FUNCTION TABLE — 'FCT157T

| Enable | Select Inputs | Data Inputs | | Output |
|---|---|---|---|---|
| $\overline{E}$ | S | $I_0$ | $I_1$ | Y |
| H | X | X | X | L |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

1738 Tbl 07

H = High voltage level
L = Low voltage level
X = Don't care

## FUNCTION TABLE — 'FCT158T

| Enable | Select Inputs | Data Inputs | | Output |
|---|---|---|---|---|
| $\overline{E}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | H |
| L | L | X | L | H |
| L | L | X | H | L |
| L | H | L | X | H |
| L | H | H | X | L |

1738 Tbl 08

## PIN DESCRIPTIONS

| Pin Names | Description |
|---|---|
| S | Common Select Input |
| $\overline{E}$ | Enable Input (Active LOW) |
| $I_{0A} - I_{0D}$ | Data Inputs from Source 0 |
| $I_{1A} - I_{1D}$ | Data Inputs from Source 1 |
| $Y_A - Y_D$ | Non-Inverted Output |
| $\overline{Y}_A - \overline{Y}_D$ | Inverted Output |

1738 Tbl 09

## AC CHARACTERISTICS ('FCT157T)

| Symbol | Parameter | 'FCT157T | | | | 'FCT157AT | | | | 'FCT157CT | | | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIL | | COM'L | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $I_n$ to Y | 1.5 | 7.0 | 1.5 | 6.0 | 1.5 | 5.8 | 1.5 | 5.0 | 1.5 | 5.0 | 1.5 | 4.3 | ns | 1, 3 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{E}$ to Y | 1.5 | 12.0 | 1.5 | 10.5 | 1.5 | 7.4 | 1.5 | 6.0 | 1.5 | 5.9 | 1.5 | 4.8 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay S to Y | 1.5 | 12.0 | 1.5 | 10.5 | 1.5 | 8.1 | 1.5 | 7.0 | 1.5 | 6.0 | 1.5 | 5.2 | ns | 1, 3 |

**Note:** Minimum limits are guaranteed but not tested on Propagation Delays.

1738 Tbl 10

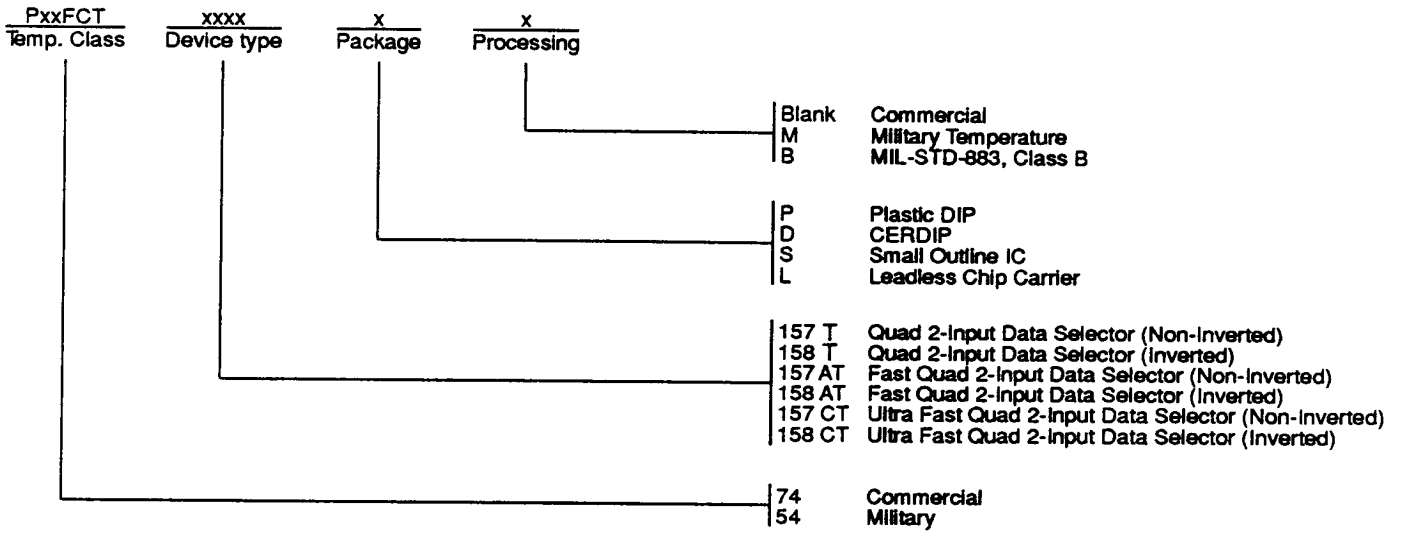
## AC CHARACTERISTICS ('FCT158T)

| Symbol | Parameter | 'FCT158T | | | | 'FCT158AT | | | | 'FCT158CT | | | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIL | | COM'L | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | Min.[1] | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $I_n$ to Y | 1.5 | 7.5 | 1.5 | 6.5 | 1.5 | 6.3 | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 4.8 | ns | 1, 2 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{E}$ to Y | 1.5 | 12.5 | 1.5 | 11.0 | 1.5 | 7.9 | 1.5 | 6.5 | 1.5 | 6.4 | 1.5 | 5.3 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay S to Y | 1.5 | 12.5 | 1.5 | 11.0 | 1.5 | 8.6 | 1.5 | 7.5 | 1.5 | 6.5 | 1.5 | 5.7 | ns | 1, 2 |

**Note:** Minimum limits are guaranteed but not tested on Propagation Delays.

1738 Tbl 11

## ORDERING INFORMATION




1738 07