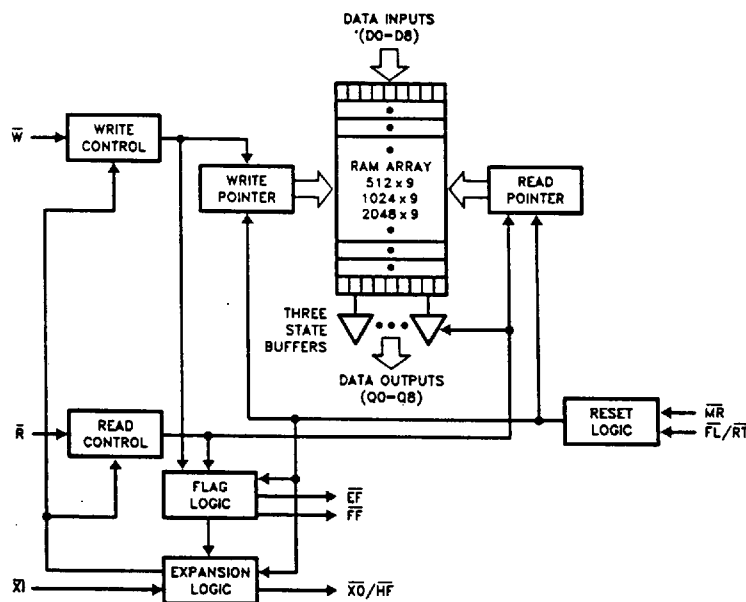


2048 x 9-Bit FIFO - Radiation Hardened 7203ERP

CMOS epi Parallel
Cascadeable FIFO

*For Space
Applications*

SEI's 7203ERP (RP for RAD-PAK®) high speed FIFO microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 7203ERP is fully equivalent to the commercial 7203 (IDT) and the CY7C429 (Cypress Semiconductor). It is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner. Capable of surviving space environments, the 7203ERP is ideal for satellite, spacecraft, and space probe missions. The RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. It has a 100 krad (Si) total dose survivability, mitigation of dose enhancement, and a high-rel die attachment. The 7203ERP features the same system performance and architecture as the commercial counterparts and is manufactured on an epitaxial substrate to enhance single event latchup performance. It is available in Class S packaging and screening.



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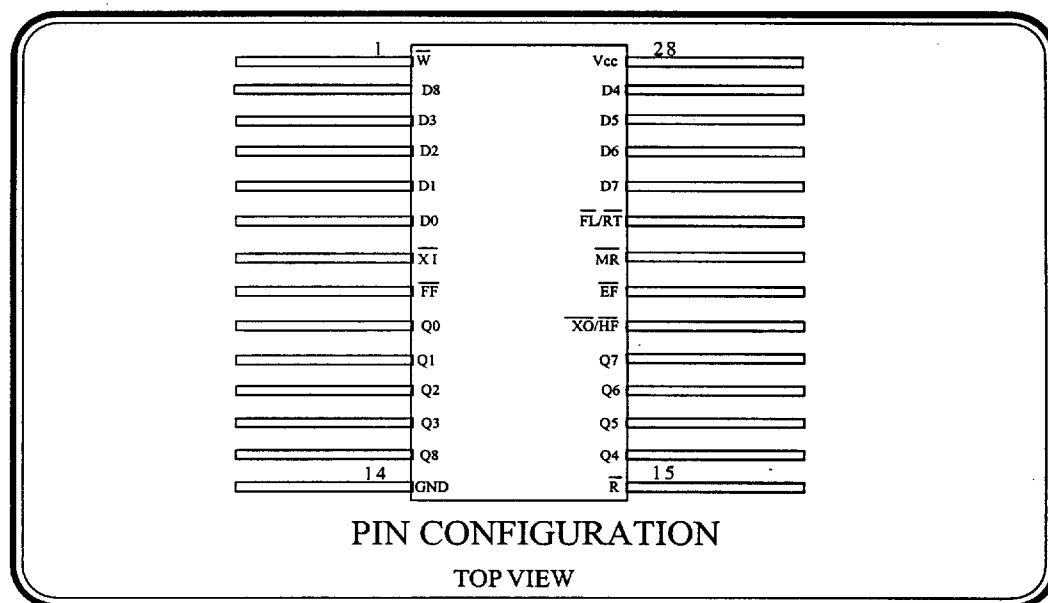
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SEI 7203ERP RAD HARD 2k x 9 FIFO MICROCIRCUIT

Radiation Hardened 7203ERP

CMOS 28 Pin
Cascadeable FIFO



Features

- 2048 x 9-bit Organization
- Pin Compatible with IDT7203/ CY7C429
- RAD-PAK® Radiation Hardened
Against Natural Space Radiation
- Epitaxial substrate for improved SEL
performance (40 MeV/mg cm²)
- Total Dose Hardness >100 krad (Si)
- Package:
 - 28 Pin RAD-PAK® flat pack
(410 mils x 720 mils)
 - Weight – 5.2 grams
 - 28 Pin RAD-PAK® DIP
(410 mils x 720 mils)
 - Weight-5.2 grams
- Fast Propagation Time (Max access time):
 - 30 ns :7203ERPx-30
 - 25 ns :7203ERPx-25
 - 20 ns :7203ERPx-20
- Asynchronous read/ write
- High Speed CMOS epi Technology
 - Half full flag in standalone
 - Empty and full flags
 - Three state outputs, TTL compatible
 - High speed 33.3 MHz read/ write
independent of depth/ width
 - Retransmit in standalone
 - Low operating power,
Icc (max) = 147 mA
- Screening per TM 5004
- QCI per TM5005

Specifications and design are subject to change without notice.



Aug. 1994

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7203ERP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{CC}	-0.5	7.0	V
DC Voltage to Outputs (During High-z State)		-0.5	7.0	V
Output Current into Outputs (Low)			20	mA
DC Input Voltage	V_{IN}	-0.5	7.0	V
Power Dissipation	P_d		1000	mW
Storage Temperature Range	T_s	-65	+150	°C
Operating Temperature Range	T_A	-55	+125	°C

7203ERP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{dd}	4.5	5.5	V
High Level Input Voltage	V_{IH}	2.2		V
Low Level Input Voltage	V_{IL}		0.8	V
Case Operating Temperature Range	T_C	-55	+125	°C



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7203ERP DC ELECTRICAL CHARACTERISTICS¹

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.2		V
Output Low Voltage $V_{CC} = 4.5 \text{ V}$, $V_{IN} = V_{IL}/V_{IH}$, $I_{OL} = 8 \text{ mA}$	V_{OL}		0.4	V
Output High Voltage $V_{CC} = 4.5 \text{ V}$, $V_{IN} = V_{IL}/V_{IH}$, $I_{OH} = -2 \text{ mA}$	V_{OH}	2.4		V
Input Low Current, $V_{IN} = 0 \text{ V}$, $V_{CC} = \text{Max}$	I_{IL}	-10	10	μA
Input High Current, $V_{IN} = 5.5 \text{ V}$, $V_{CC} = \text{Max}$	I_{IH}	-10	10	μA
Output Leakage Current, $V_{IN} = 5.5 \text{ V} / 0 \text{ V}$, $V_{CC} = \text{Max}$	I_{OZ}	-10	10	μA
Active Power Supply Current ²	I_{CC1}		147	mA
Standby Supply Current ² , ($R \setminus W \setminus RS \setminus FL \setminus VRT \setminus V_{IH}$)	I_{CC2}		12	mA
Power Down Current ² , All Input = $V_{CC} - 0.2 \text{ V}$	I_{CC3}		2	mA
Input Capacitance ³	C_{IN}		11	pF
Output Capacitance ³	C_{OUT}		15	pF

Notes:

1. $V_{CC} = 5 \pm 5\%$ volts; $T_A = -55$ to $+125^\circ\text{C}$.
2. All measurements are made with outputs open (only capacitive loading).
3. Guaranteed by design, $f = 1 \text{ MHz}$.



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7203ERP TIMING CHARACTERISTICS¹

PARAMETER	SYMBOL	MIN	MAX	UNIT
Shift Frequency 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	f_s		25 28.5 33.3	ns
Read Cycle Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RC}	40 35 30		ns
Data Access Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_A		30 25 20	ns
Read Recovery Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RR}	10 10 10		ns
Read Pulse Width ² 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RPW}	30 25 20		ns
Read LOW to Data Bus LOW ³ 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RLZ}	5 5 5		ns
Write HIGH to Data Bus Low-Z ^{3,4} 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{WLZ}	5 5 5		ns
Data Valid from Read HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{DV}	5 5 5		ns
Read HIGH to Data Bus High-Z ³ 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RHZ}		20 18 15	ns



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7203ERP TIMING CHARACTERISTICS¹ - (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{wc}	40 35 30		ns
Write Pulse Width ² 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{wpw}	30 25 20		ns
Write Recovery Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{wr}	10 10 10		ns
Data Set-up Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{ds}	18 15 12		ns
Data Hold Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{dh}	0 0 0		ns
Reset Cycle Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{rsc}	40 35 30		ns
Reset Pulse Width ² 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{rs}	30 25 20		ns
Reset Set-up Time ³ 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{rss}	30 25 20		ns
Reset Recovery Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{rsr}	10 10 10		ns



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7203ERP TIMING CHARACTERISTICS¹ - (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Retransmit Cycle Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RTC}	40 35 30		ns
Retransmit Pulse Width ² 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RT}	30 25 20		ns
Retransmit Set-up Time ³ 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RTS}	30 25 20		ns
Retransmit Recovery Time 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RSR}	10 10 10		ns
Reset to EF\ LOW 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{EFL}		40 35 30	ns
Reset to HF\ and FF\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{HFH}, t_{FFH}		40 35 20	ns
Retransmit LOW to Flags Valid 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RTF}		40 35 20	ns
Read LOW to EF\ LOW 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{REF}		30 25 20	ns
Read HIGH to FF\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RFF}		30 25 20	ns



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7203ERP TIMING CHARACTERISTICS¹ - (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Read Pulse Width after EF\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RPE}	30 25 20		ns
Write HIGH to EF\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{WEF}		30 25 20	ns
Write LOW to FF\ LOW 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{WFF}		30 25 20	ns
Write LOW to HF\ Flag LOW 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{WHF}		40 35 30	ns
Read HIGH to HF\ Flag HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{RHF}		40 35 30	ns
Write Pulse Width after FF\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{WFF}	30 25 20		ns
Read/Write LOW to XO\ LOW 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{XOL}		30 25 20	ns
Read/Write HIGH to XO\ HIGH 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{XOH}		30 25 20	ns
XI\ Pulse Width ² 7203ERP _x -30 7203ERP _x -25 7203ERP _x -20	t_{XI}	30 25 20		ns



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7203ERP TIMING CHARACTERISTICS¹ - (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNIT
XI Recovery Time	t_{XIR}			ns
7203ERP _x -30		10		
7203ERP _x -25		10		
7203ERP _x -20		10		
XI Set-up Time	t_{XIS}			ns
7203ERP _x -30		10		
7203ERP _x -25		10		
7203ERP _x -20		10		

Notes:

1. AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V and the output load circuit, unless otherwise specified.
2. Pulse widths less than minimum are not allowed.
3. Guaranteed by design, not tested.
4. Only applies to read data flow-through mode.

7203ERP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-28	28 Pin Dual In Line Package
F	F-28	28 Pin Flat Package

Note:

- 1/ For outline information, see Appendix A (Package Information - Outline Dimension)

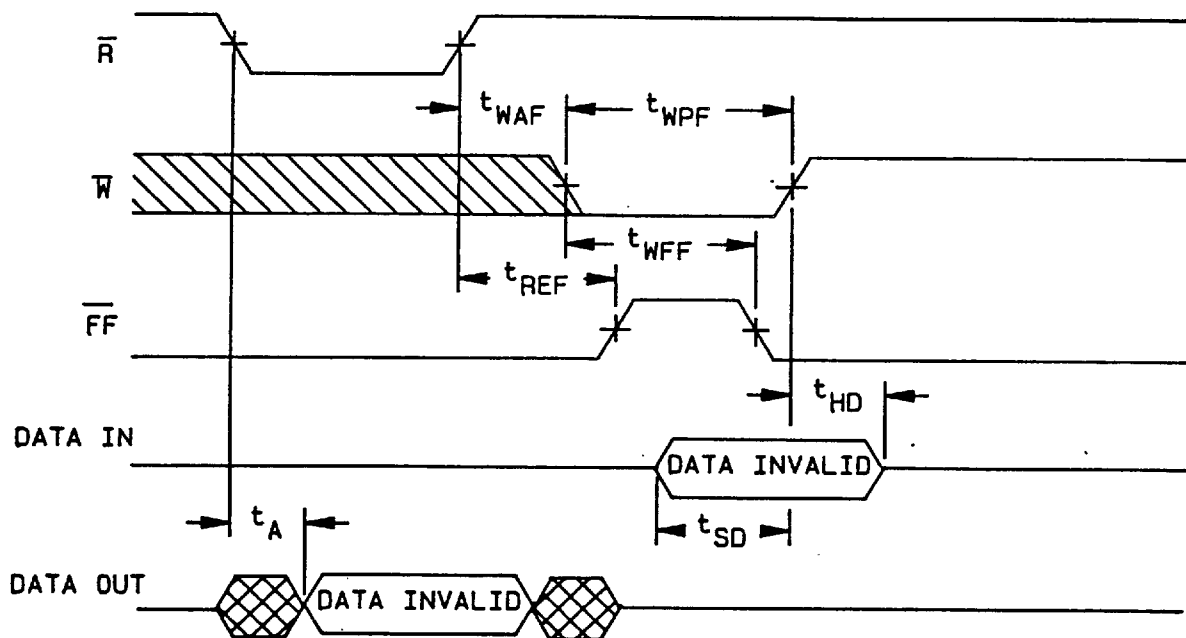


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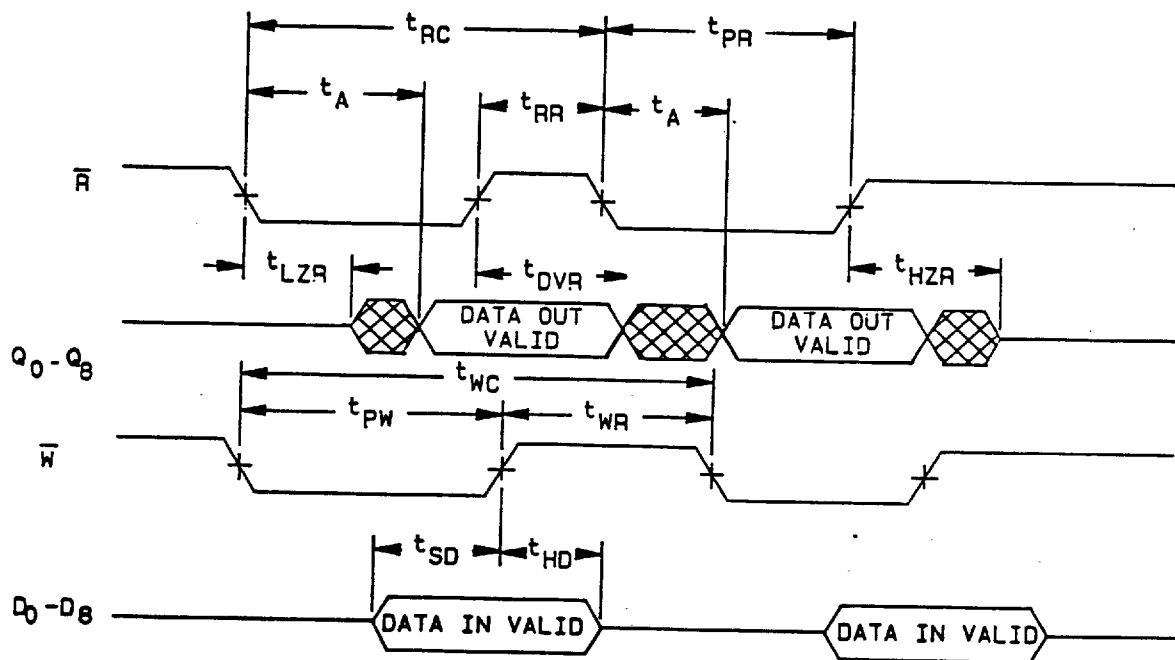
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Full Flag and Write Bubble - through Mode Timing Diagram



Asynchronous Read and Write Timing Diagram



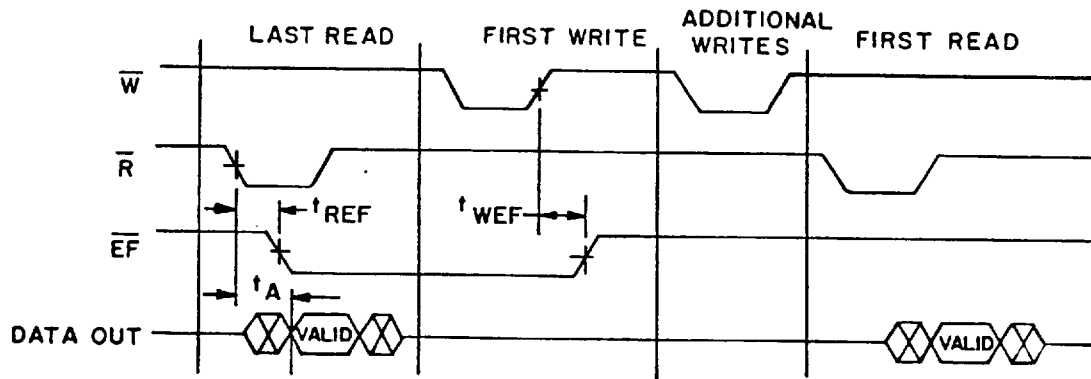
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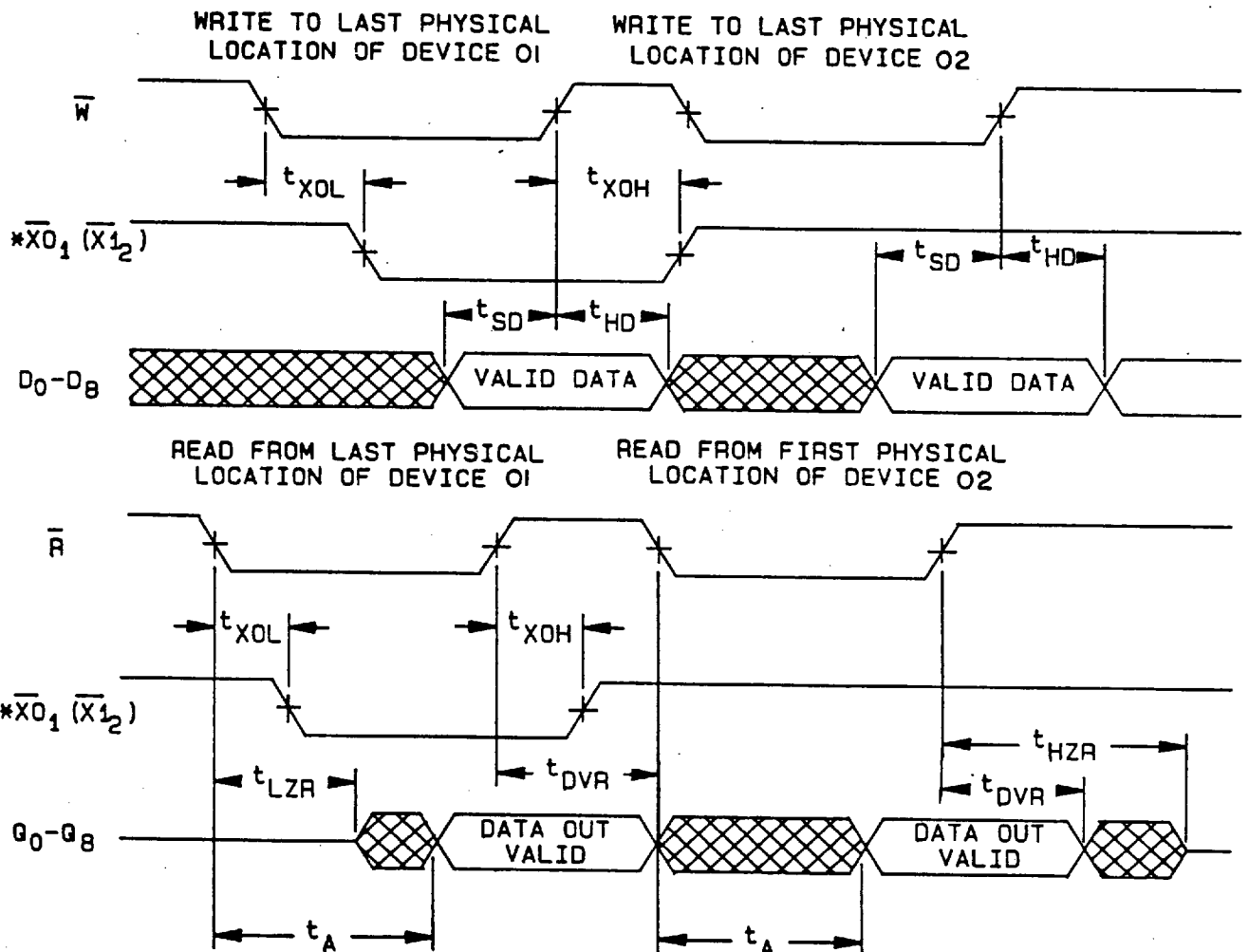
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Last Read to First Write Empty Flag Timing Diagram



Expansion Timing Diagrams

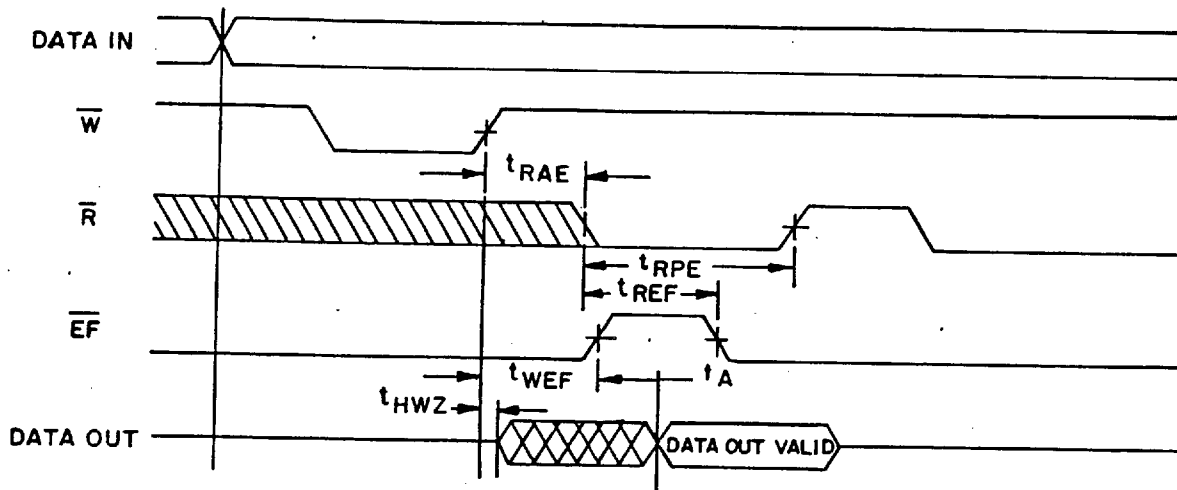


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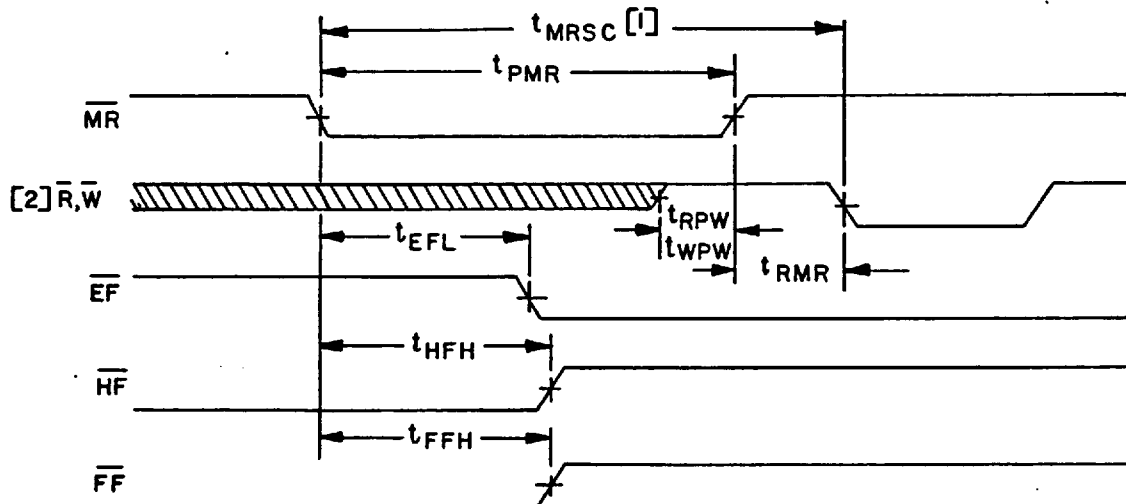
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Empty Flag and Read Bubble - through Mode Timing Diagram



Master Reset Timing Diagram



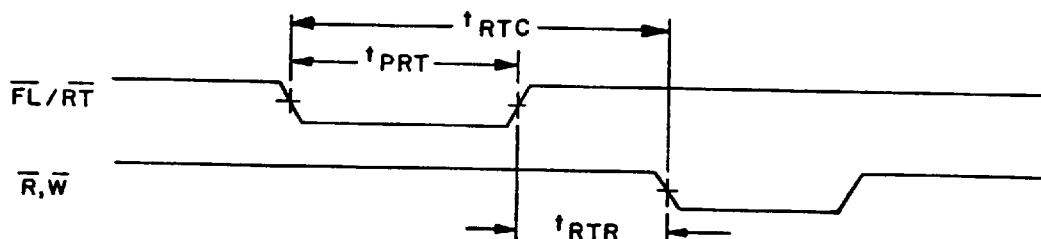
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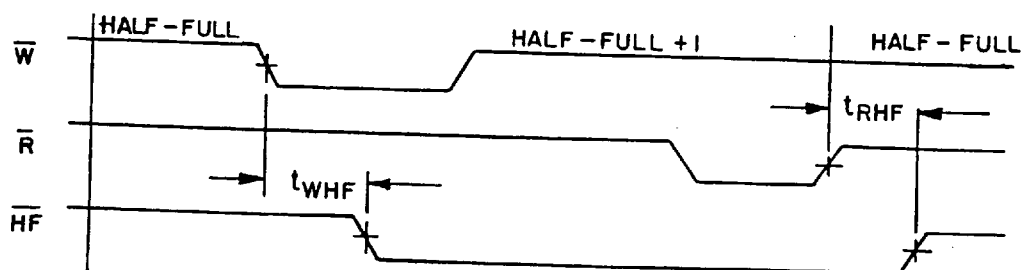
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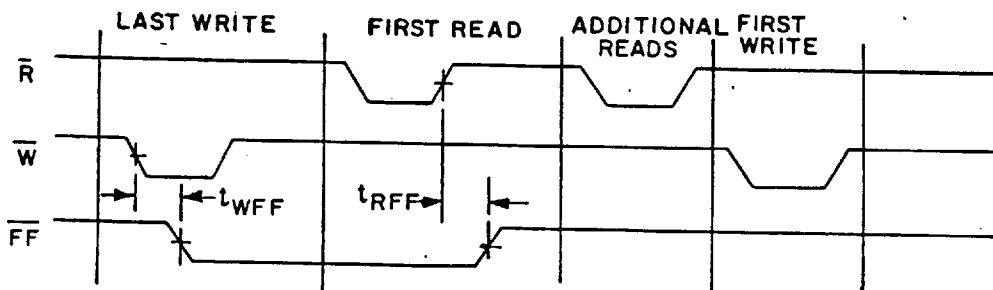
Retransmit Timing Diagram



Half - full Flag Timing Diagram



Last Write to First Read Full Flag Timing Diagram



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7203ERP PINOUT DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	W\	Write Enable
2	D8	Data Input
3	D3	Data Input
4	D2	Data Input
5	D1	Data Input
6	D0	Data Input
7	XI\	Expansion In
8	FF\	Full Flag
9	Q0	Data Output
10	Q1	Data Output
11	Q2	Data Output
12	Q3	Data Output
13	Q8	Data Output
14	GND	Ground
15	R\	Reset
16	Q4	Data Output
17	Q5	Data Output
18	Q6	Data Output
19	Q7	Data Output
20	XO\HF\	Expansion Out/ Half-Full Flag
21	EF\	Empty Flag
22	MR\	Master Reset
23	FL\RT\	First Load/ Retransmit
24	D7	Data Input
25	D6	Data Input
26	D5	Data Input
27	D4	Data Input
28	Vcc	Power Supply



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