FAIRCHILD SEMICONDUCTOR™

March 1998

100350
Low Power Hex D-Latch

General Description

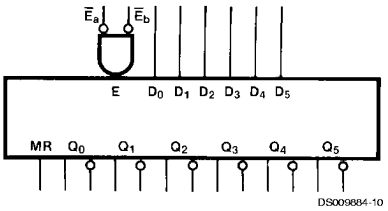
The 100350 contains six D-type latches with true and complement outputs, a pair of common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 20% power reduction of the 100150
- 2000V ESD protection
- Pin/function compatible with 100150
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code:

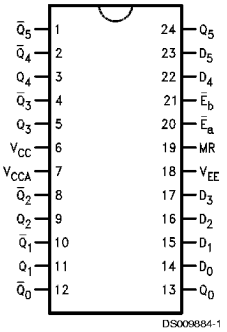
Logic Symbol



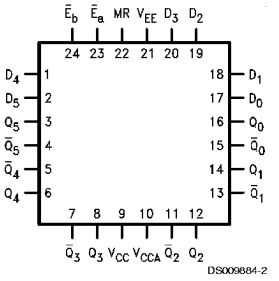
Pin Names	Description
D_0–D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP

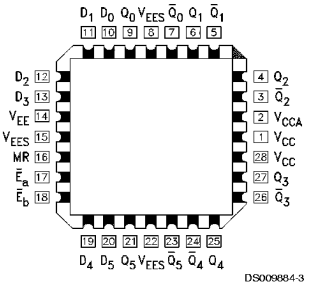


24-Pin Quad Cerpak



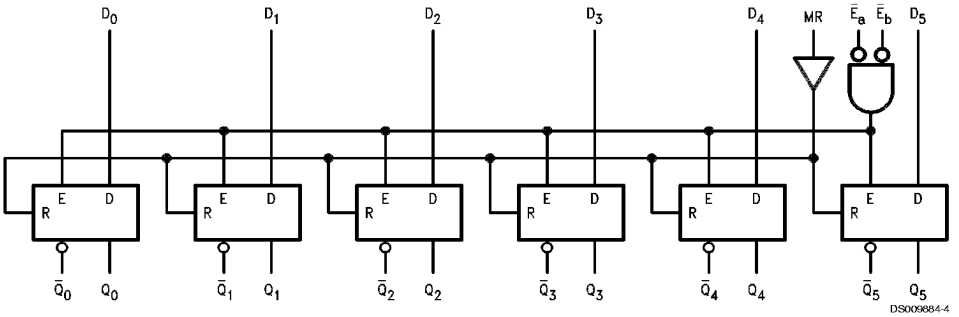
Connection Diagrams (Continued)

28-Pin PCC



DS009884-3

Logic Diagram



DS009884-4

Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched (Note 1)
X	X	H	L	Latched (Note 1)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Note 1: Retains data present before $\overline{E}$ positive transition

Asynchronous Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
X	X	X	H	L

Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 4)

V_{EE} = −4.5V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620		or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$	Loading with
V_{OLC}	Output LOW Voltage			−1610		or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current						
	MR			240			
	D_n			240	µA	V_{IN} = $V_{IH\ (Max)}$	
	$\overline{E}_a$, $\overline{E}_b$			240			
I_{EE}	Power Supply					Inputs Open	
	Current	−89		−44	mA	V_{EE} = −4.2V to −4.8V	
		−93		−44		V_{EE} = −4.2V to −5.7V	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay								*Figures 1, 2*
t_{PHL}	D_n to Output	0.50	1.40	0.50	1.40	0.50	1.50	ns	
	(Transparent Mode)								
t_{PLH}	Propagation Delay	0.75	1.85	0.75	1.85	0.75	2.05	ns	
t_{PHL}	$\overline{E}_a$, $\overline{E}_b$ to Output								
t_{PLH}	Propagation Delay	0.90	2.10	0.90	2.10	0.90	2.10	ns	*Figures 1, 3*
t_{PHL}	MR to Output								
t_{TLH}	Transition Time	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1, 2*
t_{THL}	20% to 80%, 80% to 20%								
t_s	Setup Time								*Figures 3, 4*
	D_0–D_5	1.00		1.00		1.00		ns	
	MR (Release Time)	1.60		1.60		1.60			
t_h	Hold Time, D_0–D_5	0.40		0.40		0.40		ns	*Figure 4*

DIP AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.20	0.50	1.20	0.50	1.30	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.65	0.75	1.65	0.75	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	1.90	0.90	1.90	0.90	1.90	ns	*Figures 1, 3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1, 2*
t_s	Setup Time D_0–D_5	0.90		0.90		0.90		ns	*Figures 3, 4*
	MR (Release Time)	1.50		1.50		1.50			
t_h	Hold Time, D_0–D_5	0.30		0.30		0.30		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH}(Max) or V_{IL}(Min)	Loading with 50Ω to −2.0V	(Notes 5, 6, 7)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH}(Min) or V_{IL}(Min)	Loading with 50Ω to −2.0V	(Notes 5, 6, 7)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		(Notes 5, 6, 7, 8)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		(Notes 5, 6, 7, 8)
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 5, 6, 7)

DC Electrical Characteristics (Continued)

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = –55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
I_{IH}	Input HIGH Current						(Notes 5, 6, 7)
	MR		300				
	D_n		250	µA	0°C to +125°C		
	$\overline{E}_a$, $\overline{E}_b$		520			V_{EE} = –5.7V	
	MR		450			V_{IN} = V_{IH} (Max)	
	D_n		350	µA	–55°C		
	$\overline{E}_a$, $\overline{E}_b$		750				
I_{EE}	Power Supply Current	–138	–64	mA	–55°C to +125°C	Inputs Open	(Notes 5, 6, 7)

Note 5: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 6: Screen tested 100% on each device at –55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 7: Sample tested (Method 5005, Table I) on each manufactured lot at –55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 8: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = –55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay									
t_{PHL}	D_n to Output	0.45	1.50	0.50	1.40	0.50	1.50	ns	*Figures 1, 2*	
	(Transparent Mode)									
t_{PLH}	Propagation Delay	0.75	2.05	0.75	1.85	0.75	2.05	ns		(Notes 9, 10, 11)
t_{PHL}	$\overline{E}_a$, $\overline{E}_b$ to Output									
t_{PLH}	Propagation Delay	0.80	2.40	0.90	2.40	0.90	2.60	ns	*Figures 1, 3*	
t_{PHL}	MR to Output									
t_{TLH}	Transition Time	0.45	1.70	0.45	1.60	0.45	1.60	ns	*Figures 1, 2*	
t_{THL}	20% to 80%, 80% to 20%									
t_S	Setup Time									
	D_0-D_5	0.70		0.70		0.70		ns	*Figures 1, 2*	
	MR (Release Time)	2.10		2.10		2.10				
t_H	Hold Time, D_0-D_5	0.70		0.70		0.70		ns	*Figure 4*	(Note 12)
t_{pw}(L)	Pulse Width LOW	2.00		2.00		2.00		ns	*Figure 2*	
	$\overline{E}_a$, $\overline{E}_b$									
t_{pw}(L)	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*	

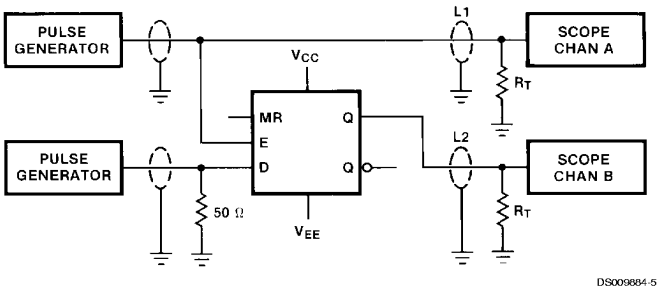
Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 11: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and –55°C temp., Subgroups A10 and A11.

Note 12: Not tested at +25°C, +125°C, and –55°C temperature (design characterization data).

Test Circuit



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

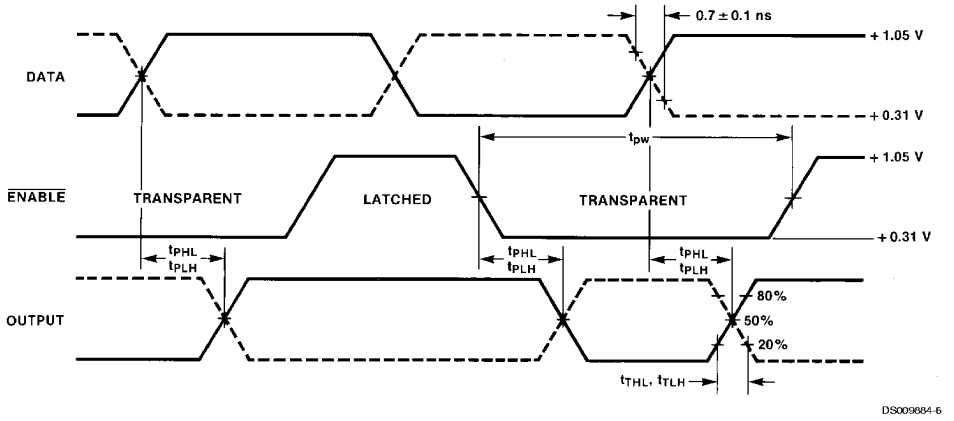


FIGURE 2. Enable Timing

Switching Waveforms (Continued)

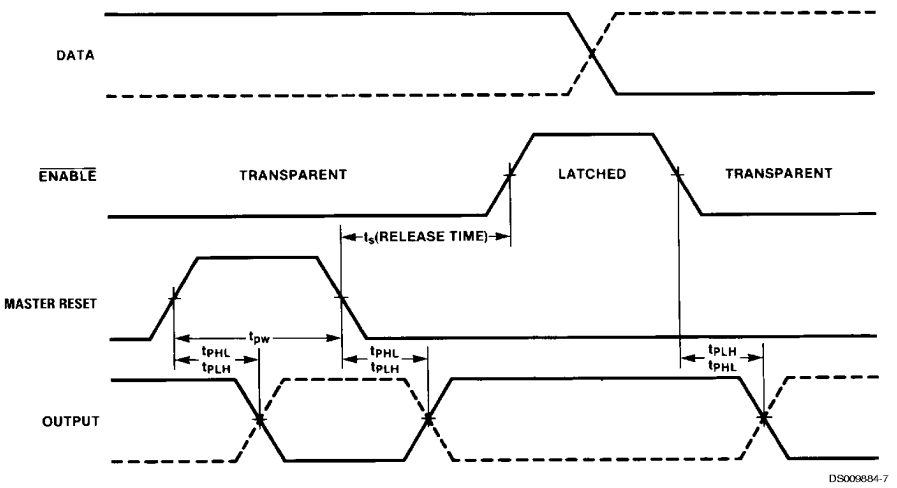
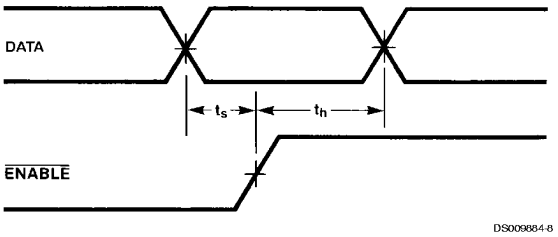


FIGURE 3. Reset Timing

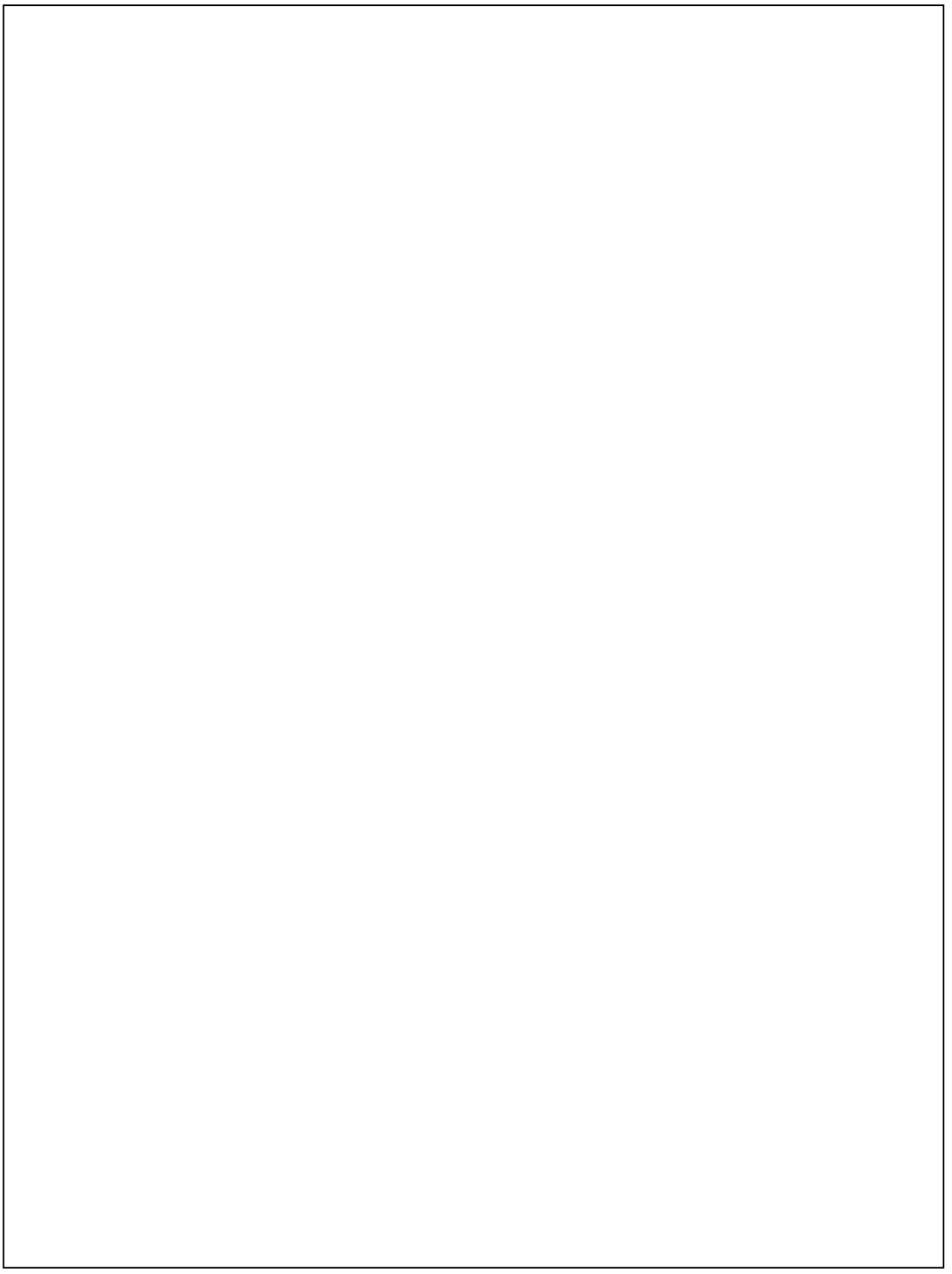


Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

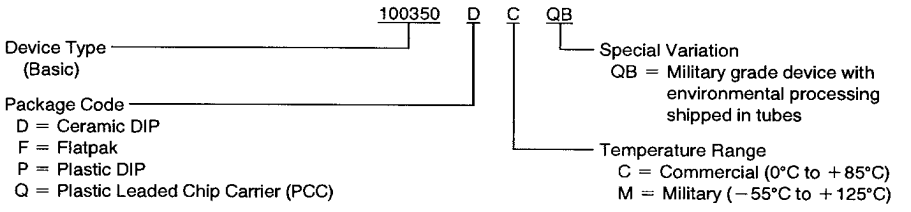
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time



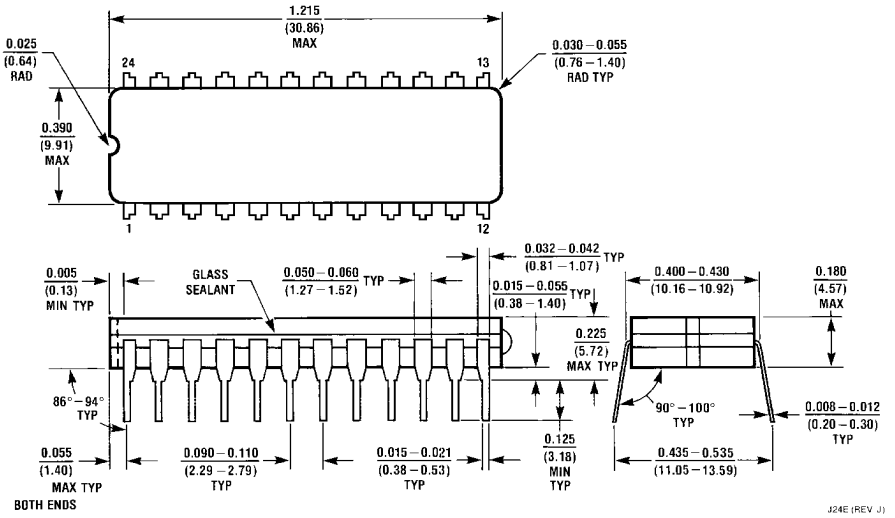
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



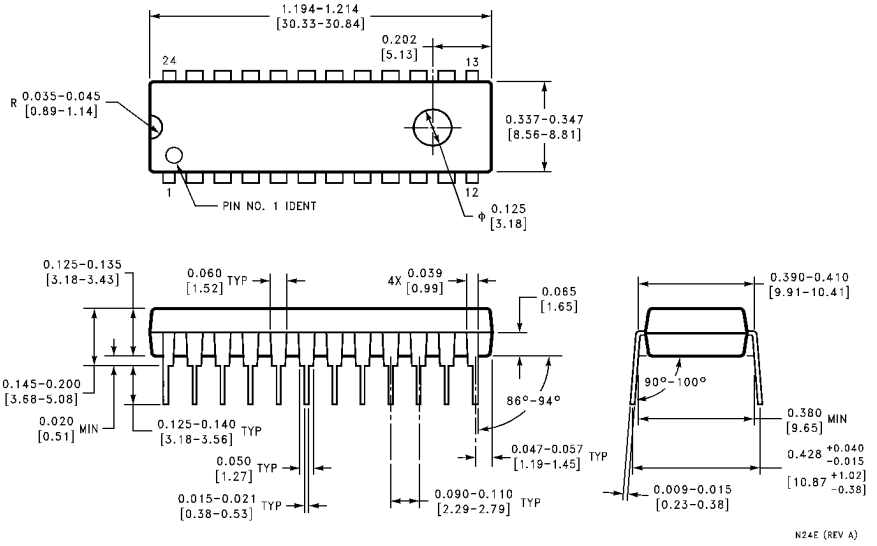
DS009884-11

Physical Dimensions inches (millimeters) unless otherwise noted



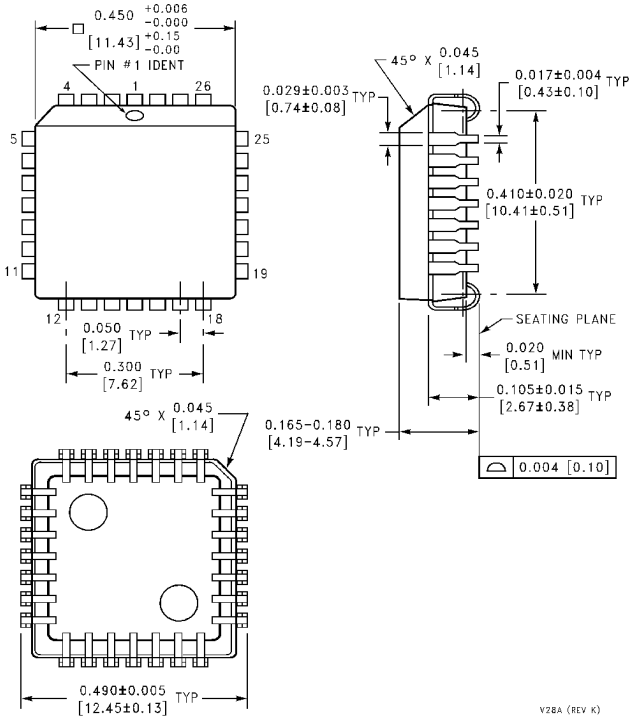
24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
Package Number J24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



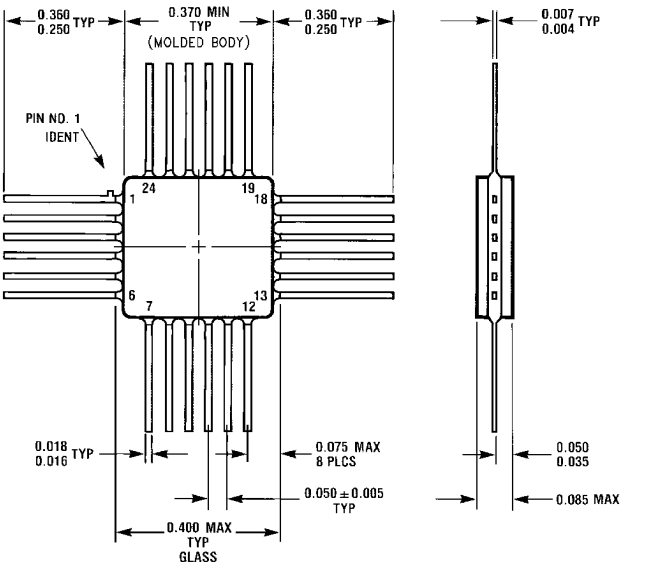
24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Chip Carrier (Q)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Quad Cerpak (F)
Package Number W24B

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com