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FAST Products	

FAST 74F393

Dual 4-Bit Binary Ripple Counter

FEATURES

- Two 4-Bit binary counters
- Two Master Resets to clear each 4-bit counter individually

DESCRIPTION

The 74F393 is a Dual Ripple Counter with separate Clock ($\overline{CP}_a$) and Master Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 'F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding. The Master Resets (MR_a and MR_b) are active High

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
14-Pin Plastic DIP	N74F393N
14-Pin Plastic SO	N74F393D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a, \overline{CP}_b$	Clock inputs	1.0/1.0	20 μ A/0.6mA
MR _a , MR _b	Master Reset inputs	1.0/1.0	20 μ A/0.6mA
Q _{na} - Q _{nb}	Data outputs	50/33.3	1.0mA/20mA

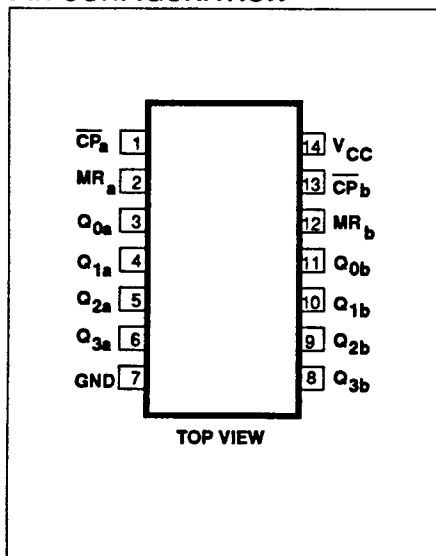
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

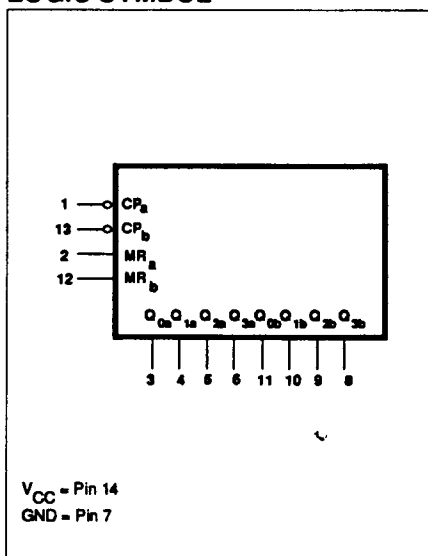
asynchronous inputs; one for each 4-bit counter. A High level in the MR input

overrides the Clock and sets the outputs Low.

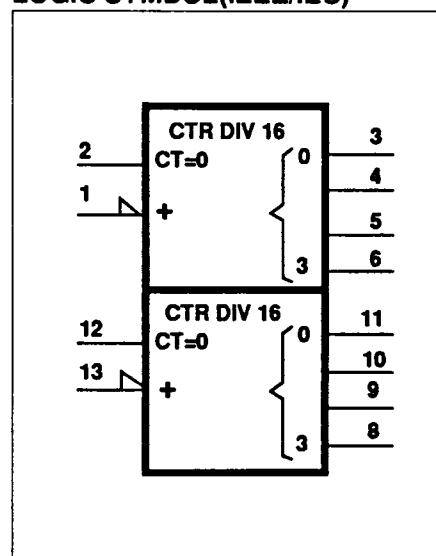
PIN CONFIGURATION



LOGIC SYMBOL



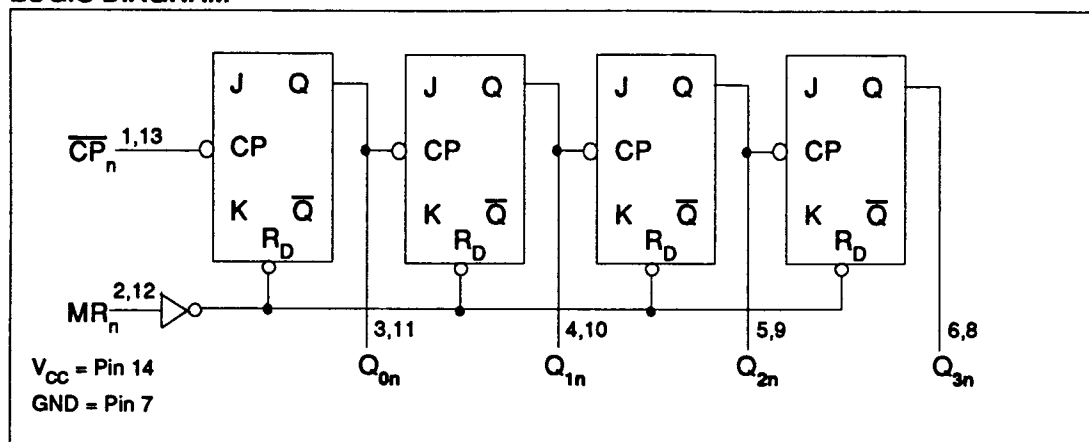
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level

L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				Min	Typ ²	Max	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$	2.5			V
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\% V_{CC}$	2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.30	0.50	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\% V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	μA
I_{ILL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		25	36	mA
		I_{CCL}			42	58	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable typ5
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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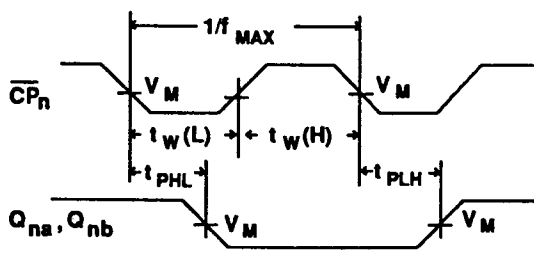
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_n$ to Q_{0a} , Q_{0b}	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0	9.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_n$ to Q_{1a} , Q_{1b}	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_n$ to Q_{2a} , Q_{2b}	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0	15.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_n$ to Q_{3a} , Q_{3b}	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5	17.0 17.5	ns
t_{PHL}	Propagation delay MR to Q_{na} , Q_{nb}	Waveform 2	4.0	6.0	9.0	4.0	9.0	ns

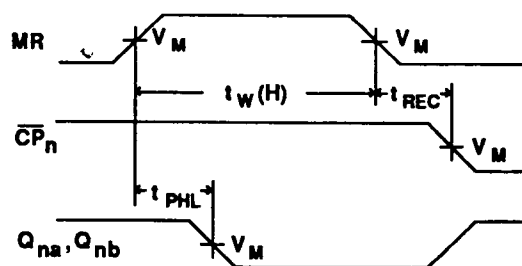
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_{w(H)}$ $t_{w(L)}$	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	4.5 3.5			5.0 4.0		ns
$t_{w(H)}$	MR Pulse width High	Waveform 2	3.5			4.5		ns
t_{REC}	Recovery time MR to $\overline{CP}_n$	Waveform 2	2.5			3.0		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

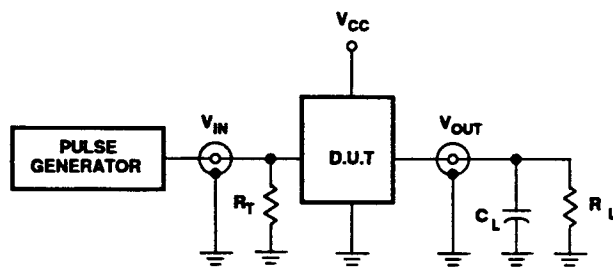
NOTE: For all waveforms, $V_M = 1.5\text{V}$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS



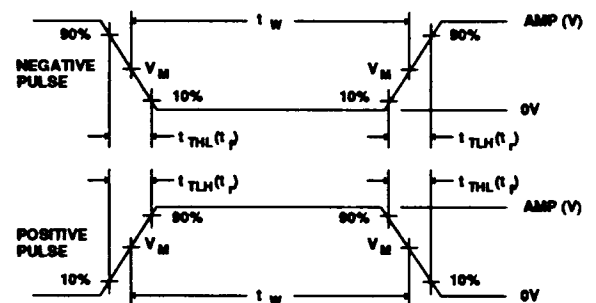
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$$V_M = 1.5V$$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns