P4C1682/P4C1682L, P4C1681/P4C1681L ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS (SCRAMS)

T-46-23-08

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FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 12/15/20/25/35 ns (Commercial)
  - 20/25/35/45 ns (Military)
- Low Power Operation (Commercial/Military)
  - 690 mW Active – 12, 15
  - 550/660 mW Active – 20/25/35/45
  - 193/220 mW Standby (TTL Input)
  - 83/110 mW Standby (CMOS Input) P4C1682/81
  - 1.1/5.5 mW Standby (CMOS Input) P4C1682L/81L
- Single Power Supply
  - 5V ± 10%
- Data Retention with 2.0V Supply, 0.5µA Typical Current
- Separate Inputs and Outputs
  - P4C1681/L Input Data at Outputs during Write
  - P4C1682/L Outputs in High Z during Write
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
  - 24-Pin 300 mil DIP
  - 24-Pin 300 mil SOIC

DESCRIPTION

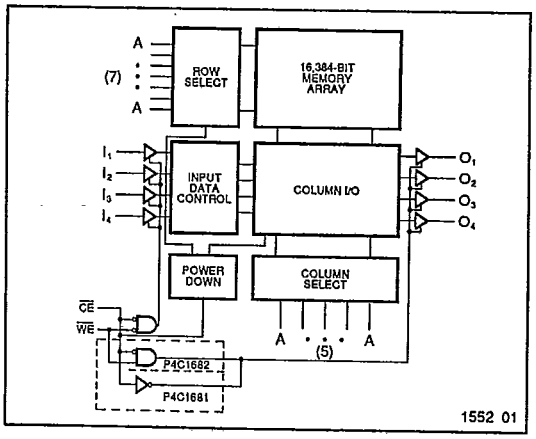
The P4C1682/L and P4C1681/L are 16,384-bit (4K x 4) ultra high speed static RAMs similar to the P4C168, but with seperate data I/O pins. The P4C1681/L features a transparent write operation; the outputs of the P4C1682/L are in high impedance during the write cycle. All devices have low power standby modes. The RAMs operate from a single 5V ± 10% tolerance power supply. With battery backup, the data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 0.5 µA from a 2.0V supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds.

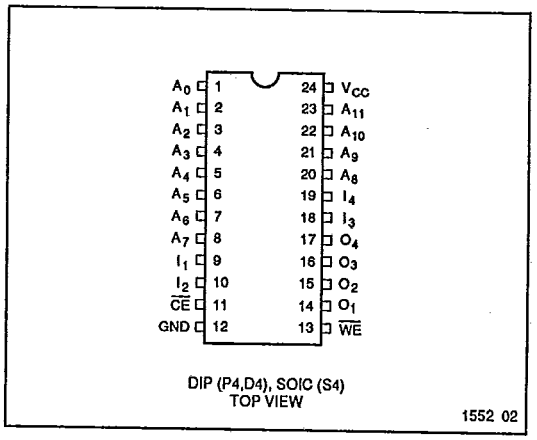
CMOS is utilized to reduce power consumption to a low 660 mW active, 193 mW standby. For the P4C1682L and P4C1681L, power is only 1.1 mW standby with CMOS input levels. The P4C1682/L and P4C1681/L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C1682/L and P4C1681/L are manufactured with PACE Technology™.

The P4C1682/L and P4C1681/L are available in 24-pin 300 mil DIP and SOIC packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

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Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Sym.	Parameter	Test Conditions		P4C1681 P4C1682		P4C1681L P4C1682L		Unit
				Min	Max	Min	Max	
V_{IH}	Input High Voltage			2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage			–0.5[3]	0.8	–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC}–0.2	V_{CC}+0.5	V_{CC}–0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage			–0.5[3]	0.2	–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +10 mA, V_{CC} = Min. I_{OL} = +8 mA, V_{CC} = Min.			0.5 0.4		0.5 0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.			0.2		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.		2.4		2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.		V_{CC}–0.2		V_{CC}–0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 –2	+5 +2	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}_1$, $\overline{CE}_2$ = V_{IH} V_{OUT} = GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 –2	+5 +2	µA

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CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

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Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C1681 P4C1682 Min	P4C1681 P4C1682 Max	P4C1681L P4C1682L Min	P4C1681L P4C1682L Max	Unit
I_{CC}	Dynamic Operating Current – 12, 15	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	n/a	—	n/a	mA
			Com'l.	—	125	—	n/a	
I_{CC}	Dynamic Operating Current – 20, 25, 35, 45	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	120	—	120	mA
			Com'l.	—	100	—	100	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., f = Max., Outputs Open	Mil.	—	40	—	40	mA
			Com'l.	—	35	—	35	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, V_{CC} = Max., f = 0, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil.	—	20	—	1.0	mA
			Com'l.	—	15	—	0.2	

n/a = Not Applicable

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DATA RETENTION CHARACTERISTICS (P4C1681L and P4C1682L Only)

Symbol	Parameter	Test Condition		Min	Typ.* V_{CC}= 2.0V	Typ.* V_{CC}= 3.0V	Max V_{CC}= 2.0V	Max V_{CC}= 3.0V	Unit
V_{DR}	V_{CC} for Data Retention			2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Mil.		0.5	1.0	100	150	µA
			Com'l.		0.5	1.0	20	30	µA
t_{CDR}	Chip Deselect to Data Retention Time			0					ns
t_R†	Operation Recovery Time			t_{RC}§					ns

*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

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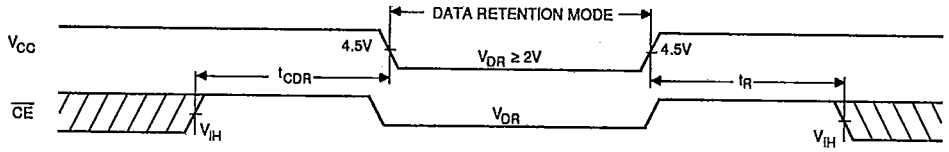
DATA RETENTION WAVEFORM



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AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-12*		-15*		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address Access Time		12		15		20		25		35		45	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45	ns
t_{OH}	Output Hold from Address Change	2		2		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		6		7		9		10		15		20	ns
t_{RCS}	Read Command Setup Time	0		0		0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		0		0		ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		25		25		30	ns

*V_{CC} = 5V ± 5% for -12, -15

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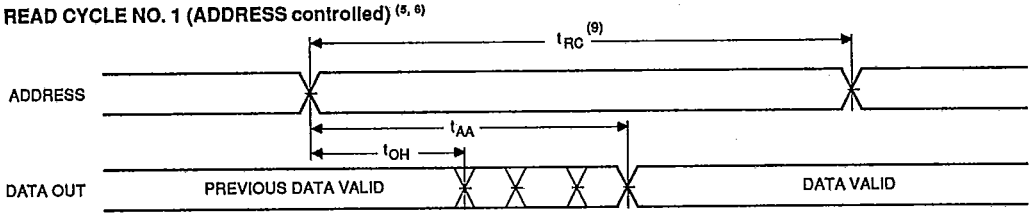
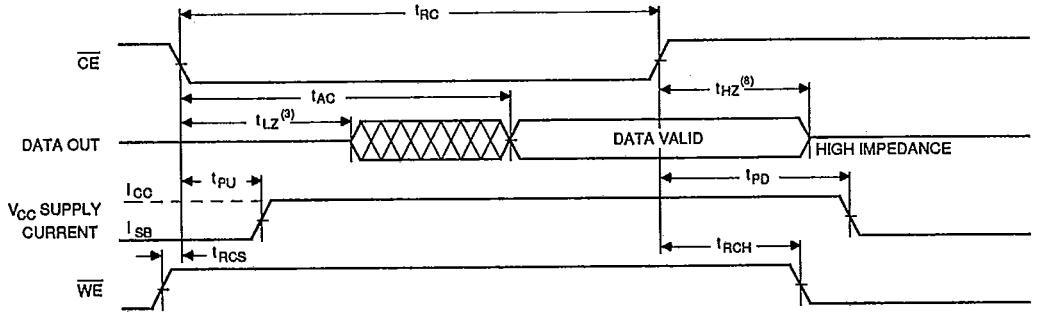
READ CYCLE NO. 1 (ADDRESS controlled) [5, 6]



1552 04

READ CYCLE NO. 2 ($\overline{CE}$ controlled) [5, 7]



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Notes:
5. $\overline{WE}$ is high for READ cycle.
6. $\overline{CE}$, $\overline{OE}$ are low for READ cycle.
7. ADDRESS must be valid prior to, or coincident with, $\overline{CE}$ transition low.
8. Transition is measured ±200mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

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(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-12*		-15*		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		15		18		20		30		40		ns
t_{CW}	Chip Enable Time to End of Write	12		15		18		20		25		35		ns
t_{AW}	Address Valid to End of Write	12		15		18		20		25		35		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		18		20		25		30		ns
t_{WR}	Write Recovery Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		8		10		10		15		15		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z†		4		5		7		7		13		20	ns
t_{OW}	Output Active to End of Write	0		0		0		0		0		0		ns
t_{AWE}	Write Enable to Data-out Valid£		12		15		20		25		30		35	ns
t_{ADV}	Data-In Valid to Data-out Valid		12		15		20		25		30		35	ns

† P4C1682/L only.
£ P4C1681/L only.
*V_{CC} = 5V ± 5% for -12, -15

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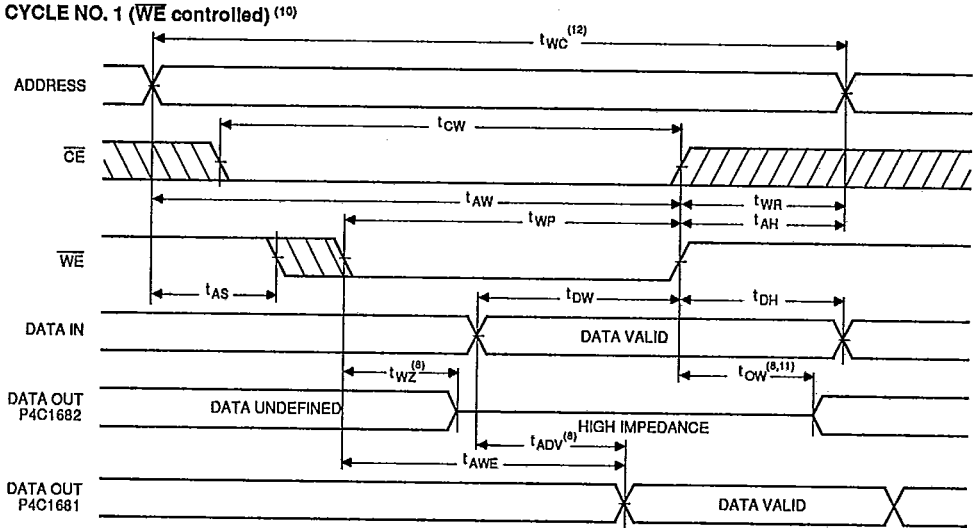
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) [10]



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10. $\overline{CE}$ and $\overline{WE}$ must be low for WRITE cycle.
11. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a low impedance state.
12. Write Cycle Time is measured from the last valid address to the first transitioning address.

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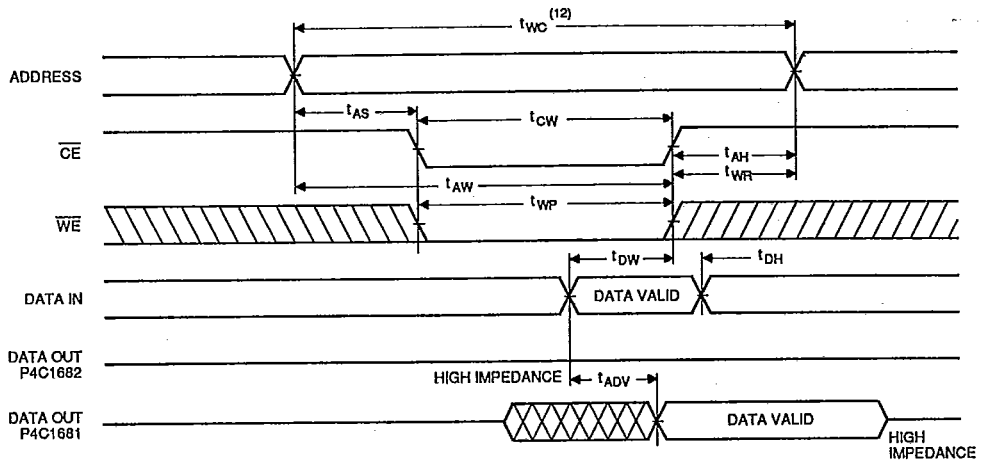
WRITE CYCLE NO. 2 ($\overline{CE}$ controlled) [12, 13]



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TRUTH TABLE

P4C1681/L (P4C1682/L)

Mode	$\overline{CE}$	$\overline{WE}$	Output
Standby	H	X	High Z
Read	L	H	DOUT
Write	L	L	DIN (High Z)

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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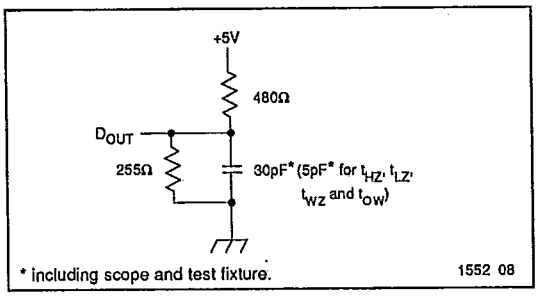

Figure 1. Output Load

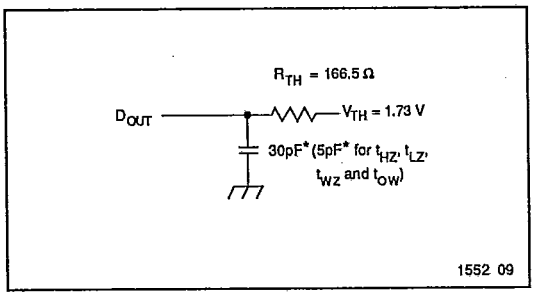

Figure 2. Thevenin Equivalent

Note:
Due to the ultra-high speed of the P4C1681/L and P4C1682/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{cc} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

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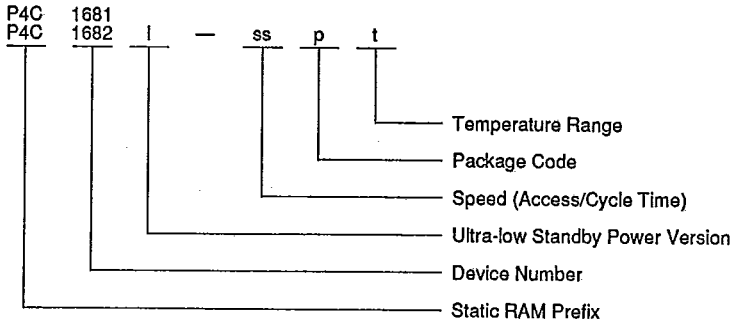

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l = Ultra-low standby power designator L, if needed.
ss = Speed (access/cycle time in ns), e.g., 25, 35
p = Package code, i.e., P, D
t = Temperature range, i.e., C, M, MB.

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PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
D	CERDIP, 300 mil wide standard
S	Small Outline IC

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

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SELECTION GUIDE

The P4C1681 and P4C1682 are available in the following temperature, speed and package options. The P4C1681L and P4C1682L are only available with access times of 20 ns and slower for commercial temperatures, 25 ns and slower for military temperatures.

Temperature Range	Speed (ns) / Package	12	15	20	25	35	45
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC	-35PC	N/A
	SOIC	–12SC	–15SC	–20SC	–25SC	–35SC	N/A
	CERDIP	N/A	-15DC	-20DC	-25DC	N/A	N/A
Military Temp.	CERDIP	N/A	N/A	-20DM	-25DM	-35DM	-45DM
Military Processed*	CERDIP	N/A	N/A	-20DMB	-25DMB	-35DMB	-45DMB

* Military temperature range with MIL-STD-883 Revision C, Class B processing.
N/A = Not available

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