Integrated
Circuit
Systems, Inc.

ICS2594

Product Preview

T-52-33-49

Dual Programmable Graphics Clock Generator

Highlights

- Pin-Compatible With Industry Standard ICS2494 Dual Graphics Clock Generator
- Ideal for High-End VGA Cards
- Sixteen ROM/RAM-based Frequency Selections for Video Clock (VCLK)
- Four ROM/RAM-based Frequency Selections for Memory Clock (MCLK)
- Extensive Power Control Features Accessible via Internal Register Bits or External Pin
- Comprehensive Output Control Features for Board Test

Features

- Advanced ICS Monolithic Phase-Locked Loop Technology
- Supports High-Resolution Graphics - VCLK/MCLK output to 135MHz

Applications

- VGA / Super VGA / XGA Video Adapters
- 8514A - TMS340X0 systems
- Workstations
- Motherboard Clock Generation

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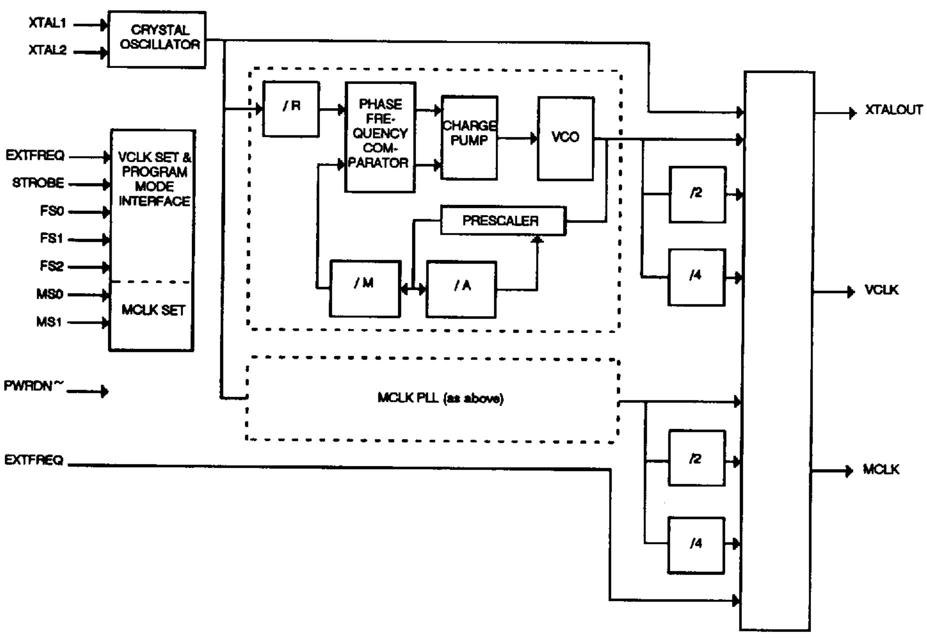
Block Diagram



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Pin Configuration

XTAL1	1	20	VDD
XTAL2	2	19	VCLK
EXTFREQ	3	18	REFOUT
VS0	4	17	RESERVED
VS1	5	16	RESERVED
STROBE	6	15	VAA
VS2	7	14	VSS
VS3	8	13	PWRDN~
MS0	9	12	MCLK
VSS	10	11	MS1

Ordering Information

ICS2594N-XXX (DIP Package)
ICS2594M-XXX (SO Package)
(XXX = Pattern number)

Product Description

The **ICS2594** is a programmable dual clock synthesizer designed to function in industry-standard graphics systems or motherboard applications. The **ICS2594** uses the latest generation of frequency synthesis techniques developed by ICS, and its performance capability is completely suitable for the most demanding system applications. It is completely compatible with the **ICS2494** ROM-based clock synthesizer, while adding several new features, the most significant of which is the ability to re-program any and all of the frequency select addresses.

Even though the **ICS2594** is a programmable part, default power-up programming is provided for each frequency select address and the Master Control Register. These pre-programmed frequencies in the ROM table of the **ICS2594** may be customized at the option of the user. ICS offers several ROM patterns that cover industry-standard VGA controllers as standard options. (Consult factory for a current list.)

The **VCLK** phase-locked loop in the **ICS2594** is pre-programmed with 16 video dot clock frequencies which may be selected with the **FS0-FS3** pins. Each one of those frequencies may be re-programmed to any desired frequency by the user, via a data sequence applied to those same pins. The **STROBE** pin may be used to block response to data on the **FS0-FS3** inputs for bus-oriented application.

The **ICS2594** is pre-programmed with four memory clock frequencies which may be selected with the **MS0-MS1** pins. Each of those frequencies may be re-programmed to any new frequency as well (also using the **FS0-FS3** inputs).

In addition to its flexible frequency synthesis capability, the **ICS2594** has the provision to multiplex an external frequency source to the **VCLK** output.

A powerdown control pin permits selection of several programmable powerdown modes. The VCLK synthesizer, MCLK synthesizer, and reference oscillator may be independently shut down. If an external signal is not available to activate this function, the shutdown mode may be activated under control of an internal register bit (see Programming). Additionally, a low frequency, "keep-alive" output mode may be selected for either or both of the **VCLK** & **MCLK** outputs.

Powerdown Modes

The **ICS2594** has a very flexible powerdown capability that permits each PLL to be independently shut down and also provides independent control of the crystal oscillator. The user can:

- reduce power consumption to less than 1 microampere.
- generate a low frequency derived from the reference oscillator and pass it through to **VCLK** and/or **MCLK** outputs.
- pass an external frequency through to **VCLK** and/or **MCLK**.
- shut down one PLL and derive both **VCLK** & **MCLK** from the remaining one.

There are three control bits in the register that enable the powerdown functions:

- VSDEN - enables the capability to shut down the VCLK PLL
- MSDEN - enables the capability to shut down the MCLK PLL
- XSDEN - enables the capability to shut down the Reference Oscillator

It is important to note that to actually execute the shutdown mode that one of two additional events must occur. Either the **PWRDN~** pin must be taken low, or the PWRDWN bit in the Master Control Register must be set to a logic 1. See the section "Data Description" for the location of these control bits.

Miscellaneous Control Functions

Other capabilities accessible through the Master Control Register within the **ICS2594** include:

- the ability to individually tri-state any/all of the outputs (**VCLK, MCLK, XTALOUT**).
- the ability to individually stop any/all of the outputs at either logic level.
- the ability to use the **EXTFREQ** input as the reference frequency source for either PLL (rather than the **XTAL1** input).
- the ability to independently control the source/sink current for each output driver.

VCLK Output Frequency Selection

The FS0-FS3 pins and the STROBE pin are used to select the desired operating frequency of the **VCLK** output from the 16 pre-programmed/user-programmed selections in the **ICS2594**. The **FS0-FS3** and **STROBE** pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the **FS0** through **FS3** inputs are transparent, that is, they directly access the **ICS2594** internals. The synthesizer will output the new frequency programmed into the location addressed by the **FS0-FS3** pins after a brief delay (see timeout specifications).

Latched Mode - When the **STROBE** pin is held LOW, the **FS0-FS3** pins are ignored. The synthesizer will output the frequency corresponding to the state of the **FS0-FS3** pins when the **STROBE** pin was last HIGH. In the event that the **ICS2594** is powered-up with the **STROBE** pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e. the one selected with **FS0** through **FS3** at a logic LOW level).

MCLK Output Frequency Selection

The **MS0-MS1** pins are used to directly select the desired operating frequency of the **MCLK** output from the four pre-programmed/user-programmed selections in the **ICS2594**. The **MS0-MS1** pins are each equipped with a pull-up and will be at a logic HIGH level when not connected. These pins are not latched with the **STROBE** input pin as the **FS0-FS3** are.

Programming Mode Selection

Because the **FS0-FS3** lines serve the dual purpose of frequency selection and programming, a sequence is required to activate the programming mode.

First, select the frequency that is to be maintained on the **VCLK** output with the **FS0-FS3** lines. As noted above, wait at least 1 millisecond to insure that the frequency change takes place (see timeout specifications).

Next, perform the following operations in sequence:

1) set **FS2** & **FS3** to a logic high level.
2) toggle the **FS3** line (i.e. high-low-high) at least five times.
3) place each new bit of programming data on the **FS2** line and toggle the **FS3** line. The new data will be latched on the rising edge of **FS3**.

In the event that the programming is not completed within approximately 1 millisecond, the programming sequence is aborted and the **FS0-FS3** inputs will again be treated as address selection data.

Programming Data Sequence

The programming data must be loaded into the **ICS2594** in the following sequence:

1) start bit (logic 0)
2) location control bits (LCB) - 5 bits
3) data (28 bits)

Location Control Bits

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

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Table 1 - Location Control Bit Programming

LCB[4-0]	LOCATION
00000	VCLK Address 0
00001	VCLK Address 1
00010	VCLK Address 2
00011	VCLK Address 3
00100	VCLK Address 4
00101	VCLK Address 5
00110	VCLK Address 6
00111	VCLK Address 7
01000	VCLK Address 8
01001	VCLK Address 9
01010	VCLK Address 10
01011	VCLK Address 11
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10000	MCLK Address 0
10001	MCLK Address 1
10010	MCLK Address 2
10011	MCLK Address 3
11111	Master Control Register

Data (VCLK/MCLK Addresses):

When a **VCLK** or **MCLK** address has been selected by the Location Control Bits shown above, the Data Bits control ICS2594 function for that address according to the table shown here. Bit 0 is sent first, Bit 26 last.

Table 2 - VCLK/MCLK Frequency Programming

DATA	DESCRIPTION
0	R0
1	R1
2	R2
3	R3
4	R4
5	R5
6	R6
7	A0
8	A1
9	A2
10	reserved (set to 0)
11	M0
12	M1
13	M2
14	M3
15	M4
16	M5
17	reserved (set to 0)
18	DBLFREQ
19	V0
20	V1
21	V2
22	S0
23	S1
24	S2
25	reserved (set to 0)
26	reserved (set to 0)
27	reserved (set to 0)

Data (Master Control Register only):

When the Master Control Register has been selected by the Location Control Bits described above, the Data Bits control overall **ICS2594** function according to the table shown here. Bit MCR[0] is sent first, Bit MCR[27] last.

Table 3 - Master Control Register Programming

MCR BIT	DESCRIPTION
0	VSDEN (1 = VCLK PLL shutdown)
1	MSDEN (1 = MCLK PLL shutdown)
2	XSDEN (1 = Ref. Oscillator shutdown)
3	PWRDWN (1 = powerdown mode)
4, 5	VCLK_D0, VDLK_D1 (control of VCLK driver) 00 = normal, 01 = high, 10 = low
6, 7	MCLK_D0, MCLK_D1 (control of XTALOUT driver, as above)
8, 9	XTAL_D0, XTAL_D1 (control of XTALOUT driver, as above)
10	VCLK SRCI (1 = high source current)
11	VCLK SNKI (1 = high sink current)
12	MCLK SRCI (1 = high source current)
13	MCLK SNKI (1 = high sink current)
14	XTAL SRCI (1 = high source current)
15	XTAL SNKI (1 = high sink current)
16	VCLK REF (0 = XTAL1, 1 = EXTFREQ)
17	MCLK REF (0 = XTAL1, 1 = EXTFREQ)
18-20	XTALOUT Source Select (see Table)
21-27	t.b.d.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS2594**. The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS2594** from an external frequency source.

The **ICS2594** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO} = F_{XTAL1} \cdot \frac{N}{R}$$

where N is the modulus of the feedback divider chain and R is the modulus of the reference divider chain.

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers). The divider programming is one of the functions performed by the programmable look-up table in the **ICS2594**.

The feedback divider makes use of a dual-modulus prescaler technique that allows the construction of a programmable counter that operates at high speeds while still allowing the feedback divider to be programmed in steps of one. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

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Programming the R, A and M Dividers

The value that must be programmed into the R divider is the desired modulus minus one. For example, if a reference oscillator divide modulus of seven is desired, set the R divider to 6_{10} (or 0001010_2).

The programming of the A and M dividers is a bit more difficult. To understand the operation of the dual-modulus prescaler, imagine for a moment the operation of a simple (single-modulus) prescaler that has a fixed value (let us say, seven). If the desired total feedback divider were 56, we would simply set the M counter for a modulus of eight. Since the M counter is only counting the output of the prescaler, the effective feedback divider modulus will be ($8 \cdot 7 = 56$). If we wanted to achieve an effective feedback divide modulus of 55, however, we would not be able to achieve this with a simple prescaler, as 55 is not a multiple of seven.

This is where the dual-modulus technique is valuable. In the example above (desired modulus = 55), we would switch the prescaler to a divide-by-six mode after seven output pulses from the prescaler. The resultant modulus will be 55 ($7 \cdot 7 + 6$).

See Table 7 for the recommended A and M divider programming for any possible feedback divider modulus. Note that higher values can be obtained by setting the DBLFREQ bit. This will double the value of the feedback modulus. Of course, only even integers can be obtained when this is done.

It is normally advisable to keep the output frequency of the R divider in a range of 200kHz-4MHz for best performance in video applications.

Programming the VCO Gain

The PLL design of the **ICS2594** allows the gain of the VCO to be controlled for best performance in the application. The higher the gain setting, the higher the VCO frequency capability will be. Recommended gain programming is shown below. Generally speaking, the best gain to use is the lowest one that will achieve the desired frequency.

Table 4 - VCO Gain Programming

MAXIMUM (MHz)	V[2-0]
20	000
35	001
50	010
70	011
85	100
100	101
115	110
>135	111

Output Multiplexer Programming

Each of the three outputs of the **ICS2594** may be programmed to select one of eight sources. The programming of the VCLK & MCLK outputs may be done on a location-by-location basis via the S[2-0] bits in the programming data for each location.

Table 5 - VCLK/MCLK Output Selection

OUTPUT SELECTION	MCR[2-0]
F(XTAL1)	000
VCLK PLL	001
VCLK PLL/2	010
VCLK PLL/4	011
MCLK PLL	100
MCLK PLL/2	101
MCLK PLL/4	110
EXTFREQ	111

The programming of the XTALOUT output is done in the Master Control Register by the bits MCR[20-18].

Table 6 - XTALOUT Output Selection

OUTPUT SELECTION	MCR[20-18]
F(XTAL1)	000
VCLK PLL	001
VCLK PLL/2	010
VCLK PLL/4	011
MCLK PLL	100
MCLK PLL/2	101
MCLK PLL/4	110
EXTFREQ	111

Programming Example

ICS provides an MS-DOS program to ICS2594 users to simplify calculation of dividers and programming. This can completely calculate all location data and the data for the Master Control Register. The data can be placed into a disk file. For those who need to compute the programming algorithmically, or those who want more direct control, we show a sample calculation here to illustrate the process.

Suppose that we desire the VCLK output to be the VCLK PLL and the output frequency to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

First, since the frequency is less than 65 MHz, we can operate the VCO at twice the desired frequency and make use of the post-divider. Some iteration with a computer shows that 91.446 MHz (actually 91.416 MHz, an error of only 0.03%) can be achieved with a ratio of:

$$\frac{N}{R} = \frac{83}{13}$$

The programming value for the R divider will be 13 - 1, or 12 (0001100_2).

From the table we find that the programming value for the A divider will be: 5 (101_2).

Also from the table, the programming value for the M divider will be: 12 (001100_2).

The DBLFREQ bit will be set to zero, as the feedback divider value (N above) is less than 448.

Since the VCO frequency is 100 MHz, but more than 85 MHz, we will select a VCO gain of: 6 (110_2).

Finally, since we want the VCLK output to be the VCLK PLL divided by 2, we will set the VCLK Output Select Bits (S[2-0]) to be equal to: 2 (010_2).

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Table 7 - "A" & "M" Divider Programming

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes:

To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M + 1) \cdot 6] + A$

except when A = 0, then: $N = (M + 1) \cdot 7$

Under all circumstances: $A \leq M$

Reference Oscillator & Crystal Selection

The **ICS2594** has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the **ICS2594**. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.0025-0.005%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS2594** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the **XTAL1** pin of the **ICS2594**. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated. Both the VCLK PLL and MCLK PLL may also be programmed to use the EXTFREQ input as the reference frequency source.

Power Supply

The **ICS2594** has two **VSS** pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS2594** has a **VDD** pin which is the supply of +5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the **ICS2594**.

The **VAA** pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

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Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	XTAL1	Quartz crystal connection 1/Reference Frequency Input
2	XTAL2	Quartz crystal connection 2
3	EXTFREQ	External Frequency Input
4	VS0	VCLK Frequency Select LSB
5	VS1	VCLK Frequency Select Bit
7	VS2	VCLK Frequency Select Bit
8	VS3	VCLK Frequency Select MSB
6	STROBE	Control for Latch of VCLK Select Bits (VS0-FS3)
19	VCLK	Output Frequency of VCLK Synthesizer/Post-Selector
9	MS0	MCLK Select LSB
11	MS1	MCLK Select MSB
12	MCLK	Output Frequency of MCLK Synthesizer/Post-Selector
18	REFOUT	Buffered Reference Frequency Output
13	PWRDN~	Powerdown Control Bit (Logic Low to Select Powerdown)
16, 17	RESERVED	Must Be Connected to BSS
10, 14	VSS	Device Ground. Both pins must be connected.
20	VDD	Output Stage V_{DD}
15	VAA	Synthesizer V_{DD}

DC Characteristics

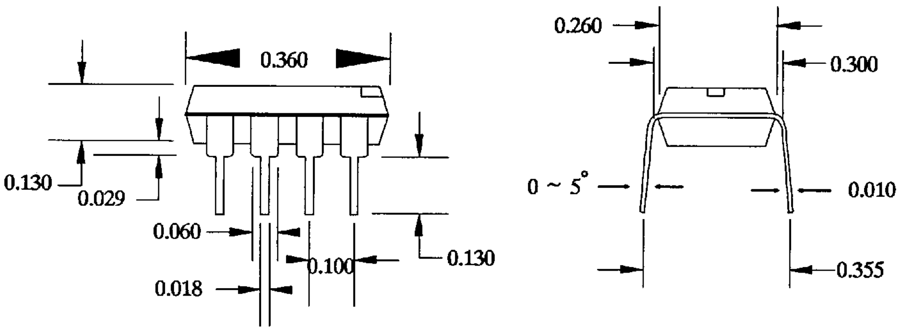
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TLL Compatible Inputs					
(VS0-3, MS0-1, STROBE):					
Input High Voltage	V_{IH}	2.0		$V_{DD}+0.5$	volts
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	volts
Input High Current	I_{IH}			10	uA
Input Low Current	I_{IL}			200	uA
Input Capacitance	C_{IN}			8	pF
XTAL 1 Input:					
Input High Voltage	V_{XH}	V_{DD}*0.7		$V_{DD}+0.5$	volts
Input Low Voltage	V_{XL}	V_{SS}-0.5		V_{DD}*0.25	volts
VCLK, MCLK Outputs:					
Output High Voltage	V_{OH}	2.4			volts
@I_{OH}=0.4mA					
Output Low Voltage	V_{OL}			0.4	volts
@I_{OL}=8.0mA					

AC Characteristics

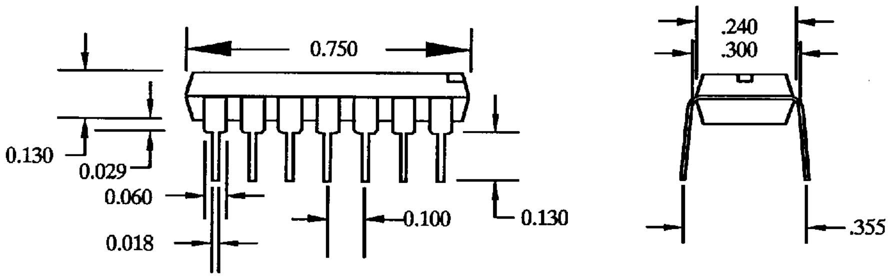
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Phase-Locked Loop:					
VCLK, MCLK VCO	F_{VCO}	20		135	MHz
PLL Acquire Time	T_{LOCK}		500		uSec
Crystal Oscillator					
Crystal Frequency Range	F_{XTAL}	5		20	MHz
Parallel Loading Capacitance			20		pF
XTAL1 Minimum High Time	T_{XHI}	8			nSec
XTAL1 Minimum Low Time	T_{XLO}	8			nSec
Input Capacitance	C_{IN}			8	pF
Power Supplies:					
VDD Supply Current	I_{DD}			35	mA
VAA Supply Current	I_{AA}			10	mA
Digital Inputs:					
	1				nSec
	2				nSec
	3				nSec
	4				nSec
Digital Outputs:					
VCLK, MCLK, XTALOUT	Tr			3	nSec
VCLK, MCLK, XTALOUT	Tf			3	nSec

T-90-20

DIP Packages



8 Pin DIP Package



14 Pin DIP Package

Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

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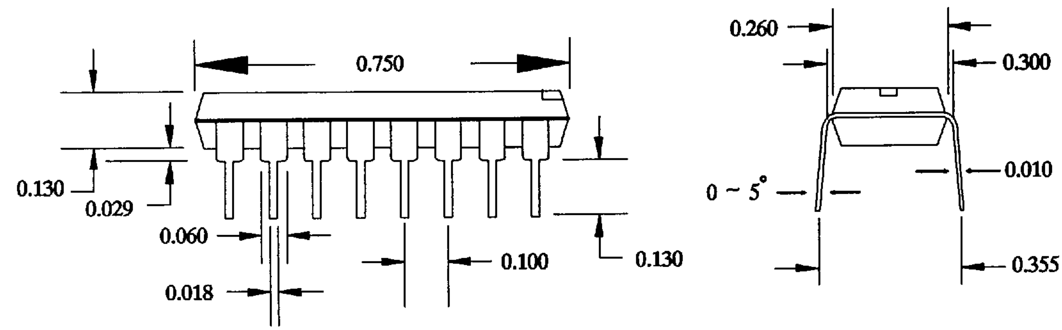
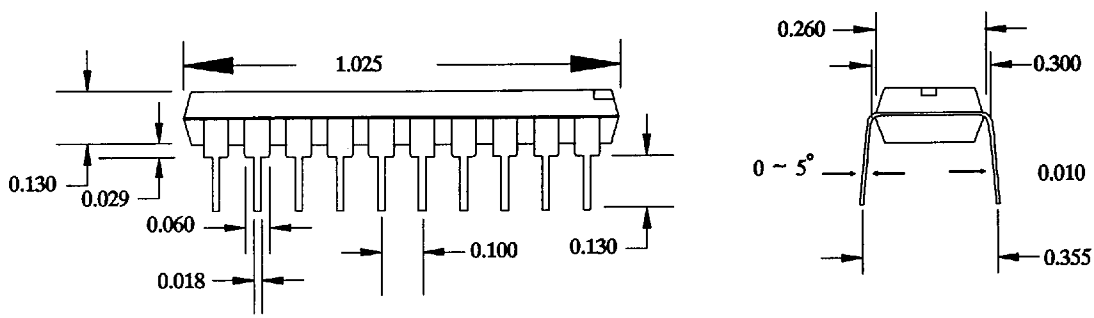
DIP Packages



16 Pin DIP Package



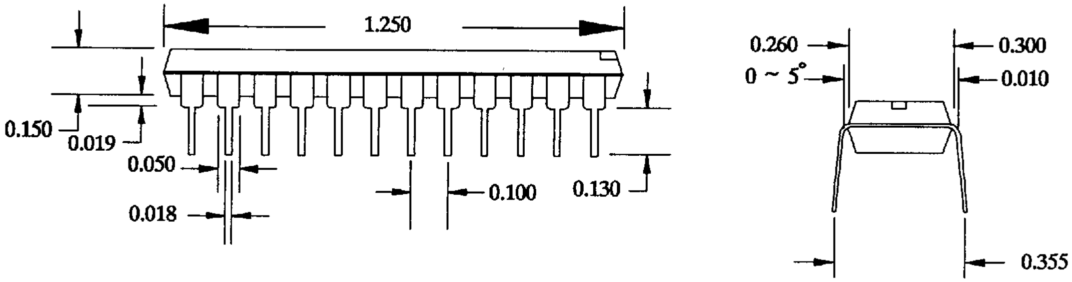
20 Pin DIP Package

Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

DIP Packages



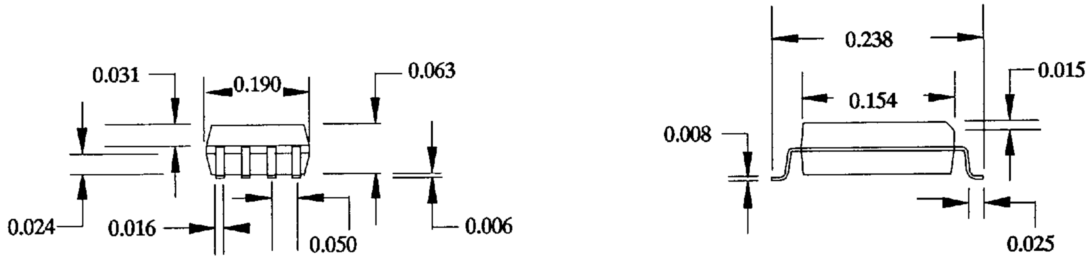
24 Pin DIP Package

Ordering Information:

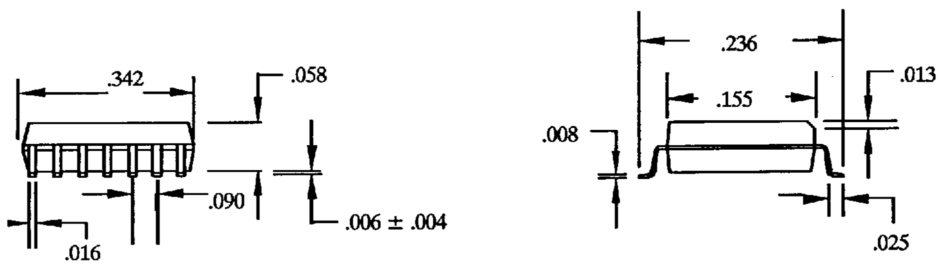
All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

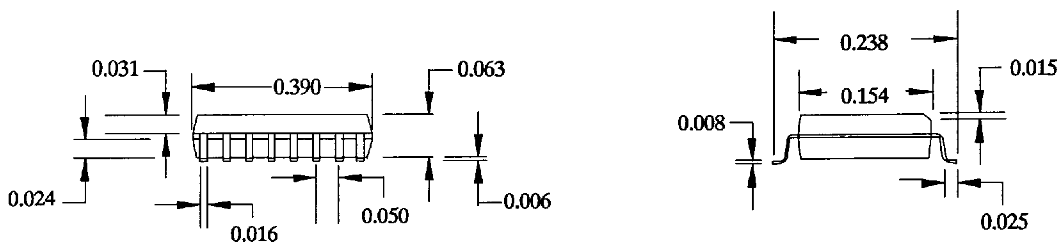
SO Packages



8 Pin SO Package



14 Pin SO Package



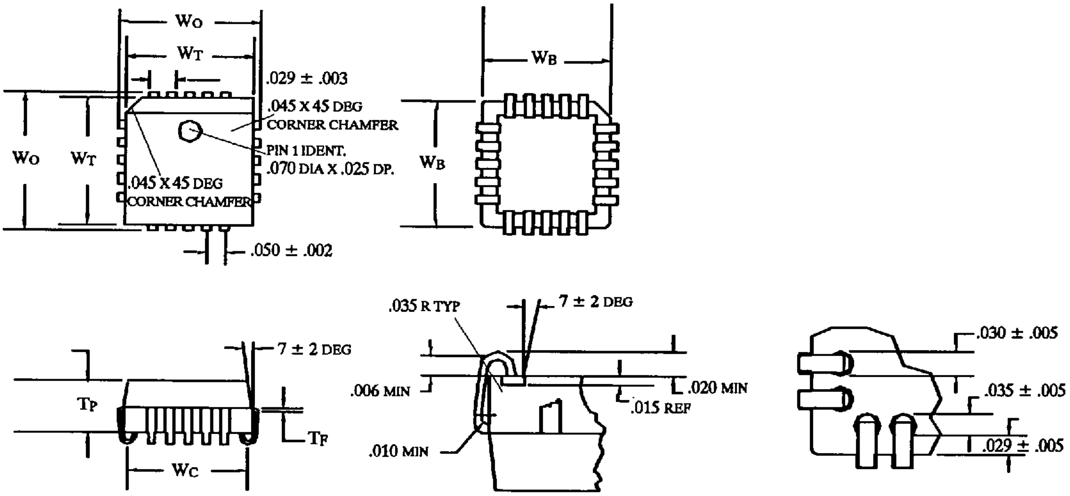
16 Pin SO Package

Ordering Information:

All ICS devices in SO packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM

PLCC Packages



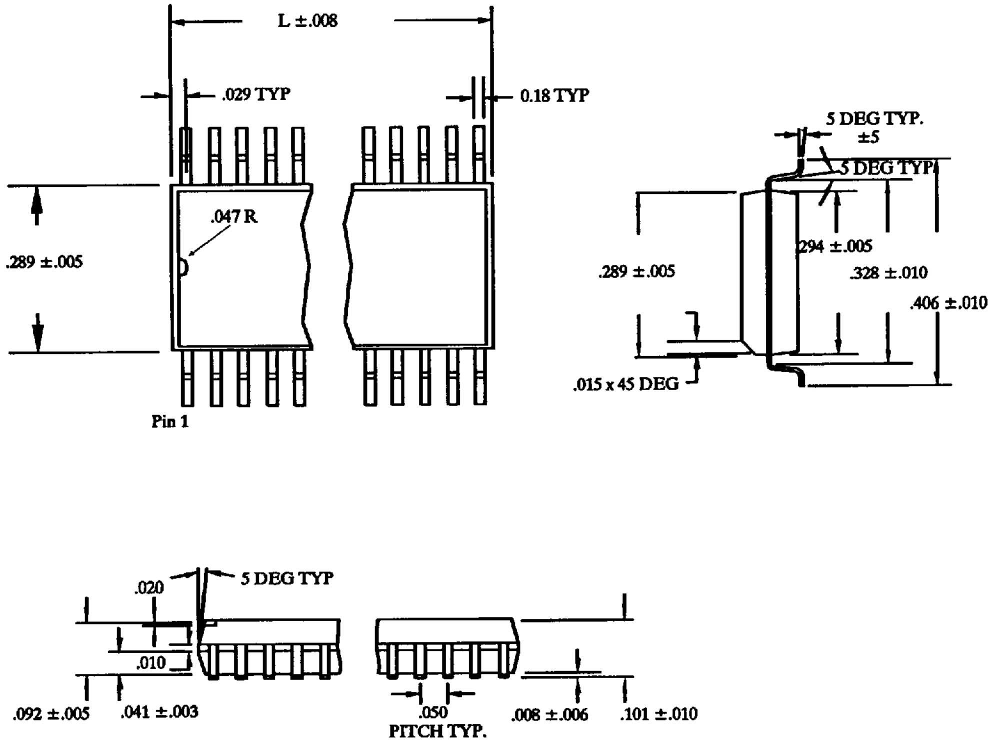
LEAD COUNT	FRAME THICKNESS TF +/-.0003	PKG. THICKNESS TP +/-.004	PKG. WIDTH TOP WT +/-.004	PKG. WIDTH BOTTOM WB +/-.066	OVERALL PKG. WIDTH WO +/-.005	CONTACT WIDTH WO +.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

Ordering Information:

All ICS devices in PLCC packages carry a "V" designation. See individual data sheets for more specific information.

Example: ICSXXXXV

SOIC Packages



SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	.354	.404	.454	.504	.604	.704	.704

Ordering Information:

All ICS devices in SOIC packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM