



Integrated
Circuit
Systems, Inc.

ICS2008

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SMPTE Time Code Receiver/Generator

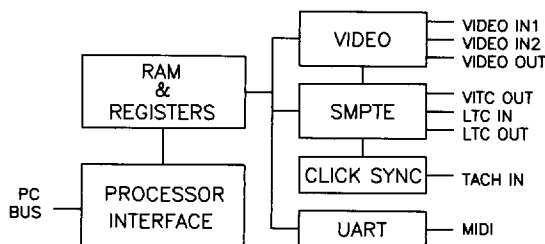
General Description

The ICS2008, SMPTE Time Code Receiver/Generator chip, is a VLSI device designed in a low power CMOS process. This device provides the timing coordination for Multimedia sight and sound events. Although it is aimed at a PC Multimedia environment, the ICS2008 is easily integrated into products requiring SMPTE time code generation and/or reception in LTC (Longitudinal Time Code) and/or VITC (Vertical Interval Time Code) formats and MTC (MIDI Time Code) translation.

Taking its input from composite video, S-Video, or an audio track, the ICS2008 can read SMPTE time code in VITC and LTC formats. Time code output formats are LTC and VITC. All are available simultaneously. A UART is provided for the user to support MTC or tape transport control.

The processor interface is compatible with the IBM PC and ISA bus compatible computers and is easily interfaced to other processors.

Block Diagram



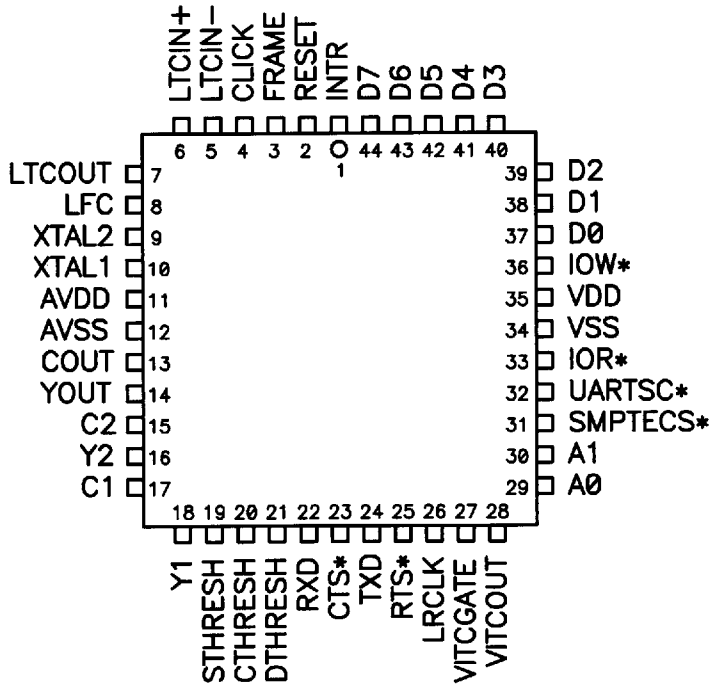
Features

- Internal and external sync sources
 - Genlock to video or house sync inputs
 - internally generated timing from oscillator input
 - external click input
- LTC and VITC Generators
 - Real Time SMPTE Rates
 - 30 Hz (B&W, some audio)
 - 29.97 Hz (NTSC)
 - 25 Hz (PAL)
 - 24 Hz (film)
 - Time Code Modes
 - Drop Frame
 - Color Frame
 - VITC can be inserted on two lines from 10-40 (SMPTE specifies lines 10-20)
 - Update all data (time code, user data, and flag bits) on a frame-by-frame basis. This allows for "Jam Sync," "freewheeling," error bypass/correction, plus-one-frame, and other intelligent generator functions.
- LTC Receiver
 - Meets SMPTE and EBU LTC specifications including drop frame, color frame, time data, user data and status bits.
 - Synchronize bit rates from 1/30th nominal to 80X nominal playback speed.
- VITC reader
 - Reads code from any or all selected scan lines.
 - Meets SMPTE VITC specifications including drop frame, color frame, time data, user data and status bits
- Time Code Burn-in Window selectable to overlay video with programmable screen position



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Package Pinout



Ordering Information:

All ICS devices in PLCC packages carry a "V" designation.

Example: ICS2008V



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Pin Description

<u>PIN</u>	<u>TYPE</u>	<u>DESCRIPTION</u>
Y1, Y2	AI	Video inputs from camera or other NTSC source. NOTE: This is also the Y (Luma) input for S-VHS and HI-8 systems.
C1, C	AI	C (Chroma) inputs for S-VHS and HI-8 systems. In NTSC systems, this pin should be tied to its respective Y input.
DTHRESH	AI	Data Threshold bypass input.
STHRESH	AI	SYNC Threshold bypass input.
CTHRESH	AI	Clamp Threshold bypass input.
YOUT	AO	NTSC video output. This is also the Y (Luma) output in S-Video mode.
COUT	AO	C (Chroma) output for S-VHS and HI-8 systems.
FRAME	AI	Color Frame A/B input. This input is self biased. (See Applications section.)
CLICK	AI	LTC SYNC input. This input is self biased. (See Applications section.)
LTCIN+	AI	SMPTE LTC input+ . This input is self biased. (See Applications section.)
LTCIN-	AI	SMPTE LTC input-. This input is self biased. (See Applications section.)
LTCOUT	AO	SMPTE LTC output.
LRCLK	O	SMPTE LTC receive clock output.
VITC	O	SMPTE VITC output to video mixer circuit.
VITCGATE	O	VITC gate indicates VITC code is being output for video overlay.
TxD	O	UART Transmit Data.
RxD	I	UART Receive Data.
CTS*	I	Clear to Send.
RTS*	O	Ready to Send.
XTAL1	I	14.318 MHz crystal input. This pin may be driven directly from a TTL 14.318 MHz source.
XTAL2	O	14.318 MHz crystal scillator output.
LFC	AI	External RC circuit.
A1-A0	I	Address bus
IOR*	I	Read Enable (active low)
IOW*	I	Write Enable (active low)
SMPTEC*	I	SMPTE port chip select (active low)
UARTCS*	I	UART chip select (active low)
RESET	I	Master reset (active high)
D7-D0	I/O	Bi-directional data bus
INTR	O	Interrupt Request (active high)
AVDD	P	Analog VDD
AGND	P	Analog Ground
VDD	P	Digital VDD
GND	P	Digital Ground

A - Analog I - Input
P - Power O - Output



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Functional Description

The following is a functional description of the hardware registers in the **ICS2008** chip. It also describes how those registers can be utilized by the software to facilitate specific application services.

Hardware Environments

The **ICS2008** operates as a peripheral to a processor such as a PC or a single chip microprocessor. Many of the real time requirements are satisfied by double buffering both incoming and outgoing time codes.

LTC Input

LTCIN is a differential analog input feeding a comparator with hysteresis. It requires capacitive coupling to the LTC source. The output of the comparator goes to the LTC receiver, which is capable of receiving LTC in a forward or backward direction at a rate from 1/30th to 80x nominal frame rates. The incoming LTC data is sampled with a phase-locked clock and loaded into the receive buffer following the receipt of a valid LTC SYNC pattern. When a complete frame has been received, an interrupt is generated.

LTC Output

The LTC output can be analog or digital. When set up as an analog output, it can drive a high impedance load.

The LTC generator outputs a LTC frame at the selected frame rate, such as 24Hz, 25Hz, 29.97Hz or 30Hz, and starts the frame based on a start time generated by the selected LTC SYNC source.

Video Inputs

There are two sets of video inputs. In a composite NTSC or PAL system, the Y input is the only one used. It is capacitively coupled to the source. In S-Video systems, capacitively couple Y and C to their respective sources. Proper termination of the source should be observed. One of the two video sources is selected by the VIDSEL bit in the SMPTE control registers as the video SYNC source. Internal timers are synchronized with the incoming video to extract timing information used to receive and generate VITC.

The VITC receiver samples the incoming video looking for a valid VITC code on selected scan lines. When a valid code is received it is written to a VITC receive buffer. More than one line can contain VITC code, and the codes can be different. For this reason, VITC codes from selected lines of a frame are written to separate VITC buffers.

Video Output

The video output combines the selected video input with the outputs from the VITC generator and the character generator. It can be a composite or an S-Video output as selected by the SVID bit in the SMPTE control registers.

VITC code is generated from data in the VITC generator buffer and output during the selected line time(s). The CRC and synchronizing bits are automatically generated by the VITC generator, but all of the data fields are sent directly from the buffer with no modification.

A character generator is provided to insert the time code in a burn-in window which overlays the incoming video. The vertical and horizontal position of the burn-in window is programmable.

MIDI Port

A UART is provided for a MIDI port. It can function as a MIDI IN and a MIDI OUT. It can generate an interrupt on receiver full and/or transmitter empty to the processor via the INTR pin. CTS and RTS modem controls are provided so that it can be used as a generic serial control port.

SMPTE SYNC Sources

A time code generator must have a SYNC input from a stable source in order to position the LTC code properly on a audio track of video tape or film. Three SYNC sources, video, click input, and free running, are available. In the case of a video tape, LTC code must start within plus or minus one line of the beginning of line 5. This requires "Genlocking" to the incoming video. The video timing section locks to the video's horizontal and vertical SYNC signal and generates a SMPTE SYNC. If some external SYNC source is available it can be input on the CLICK input. Otherwise, a free running SMPTE SYNC is generated from the oscillator at the selected frame rate.

Video Timing Generator

The video timing generator is "Genlocked" to the video input's SYNC separator. It extracts NTSC or PAL timing information from the video input and generates line and pixel rate timing for the VITC receiver, VITC generator, LTC generator and character generator. If no video input is present, it generates free running timing.



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Overlay Character Generator

It is sometimes desirable to display the time code on a video display along with the picture. A character generator is provided for that purpose. The time code display, or burn-in window, can be positioned anywhere on the screen.

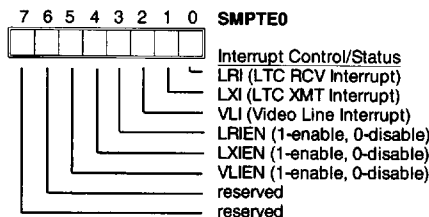
INTR Output

The INTR output pin is the interrupt source from ICS2008 to the processor. Each interrupt source has its own interrupt enable and interrupt status.

The SMPTE0 Register contains the SMPTE interrupt controls and status and the VITC read status. The three interrupt bits, LRI, LXI, VLI and TMI reflect the status of the potential interrupt sources to the processor. When a bit is set to one and the corresponding enable bit, LRIEN, LXIEN or VLIEN, is also set, the INTR output will be activated. Interrupts are cleared by reading SMPTE0. Bits 6 and 7 indicate a VITC read error. Further clarification of the error can be accomplished by reading the VITC Read Line registers, IR30 and IR31.

Processor Interface

The ICS2008 supports standard microprocessor interfaces and busses, such as the PC bus, to allow access of six control/status and data registers. These six registers are organized into two groups, one set of four for SMPTE control and the other set of two for direct UART port control. Each set of registers is selected with its own chip select, SMPTECS* and UARTCS*.



SMPTE Registers

The SMPTE register set allows access to 59 available registers. The first two are direct access registers addressed at locations 0 and 1. The remaining 64 registers are accessed by writing an indirect register address into location 2 and reading from or writing to location 3. If the AUTOINC bit in SMPTE2 is set to 1, the indirect register address is automatically incremented after an access to location 3. This eases the task of reading or writing sequential indirect locations.

LRI - This bit indicates that a LTC receive interrupt has occurred. In order for an actual processor interrupt to occur, the LRIEN bit must also be set. An LRI interrupt occurs upon reception of the last byte of LTC receive data which was preceded by a valid LTC SYNC pattern. That is after the 64th LTC receive bit time in the forward direction. At normal frame rates, if the LTC transmitter is synchronized with the LTC receiver, there is about 3 milliseconds after this interrupt before the LTC transmit data for the next output frame is transferred to the output buffer.

SMPTECS*	A1	A0	REGISTER
0	0	0	SMPTE0 Interrupt Control/Status
0	0	1	SMPTE1 SMPTE Status
0	1	0	SMPTE2 Indirect Register Address
0	1	1	SMPTE3 Indirect Register Data

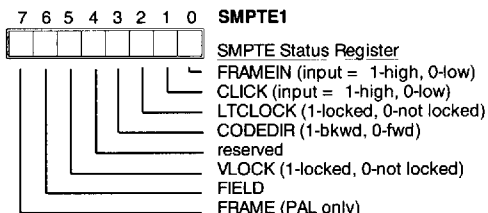
LXI - This bit indicates that a LTC transmit interrupt has occurred. When this bit is set, and the corresponding LXIEN bit has been set, the INTR output will be activated. The LTC transmit interrupt is activated after the transfer of LTC transmit data to the output buffer. This occurs after LTXEN is set to one and after the 72nd LTC transmits bit time of the current frame, "N." Data loaded after this interrupt will appear in output frame "N+ 2" since the transmitter is double buffered.

VLI - This is a status bit that indicates that the video line selected via the Video Interrupt Line Register, VR9, has passed. When the VLIEN bit is also set, the processor will be interrupted. This interrupt can be used by the processor to determine when to sample the VITC time code when time locked to a video source. It will also be used to facilitate detection of LTC time code dropout and off speed LTC code, e.g. shuttling operations.



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The SMPTE Status Register is a read only register which contains video and LTC status.



FRAMEIN - This bit indicates the state of the FRAME input pin. It is used as an alternate source for B/A frame status. This is useful when the quality of the video signal is not good enough to extract the B/A frame status.

CLICK - This bit indicates the state of the CLICK input pin. It can be used as a synchronization source for the LTC transmitter.

LTCLOCK - When a valid forward or backward LTC sync pattern is detected, this bit is set to one. It is reset to zero when an expected LTC sync pattern is missed or an invalid LTC bit is detected.

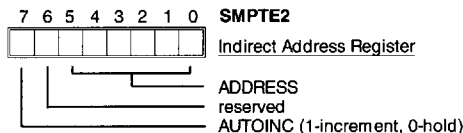
CODEDIR - The code direction bit works in conjunction with the LTCLOCK bit. When the LTCLOCK bit is set to one, the CODEDIR bit is valid. Otherwise, it is not. See the table below.

LTCLOCK	CODEDIR	LTC RECEIVER STATUS
0	X	Looking for SYNC pattern
1	0	receiving LTC (FORWARD)
1	1	receiving LTC (BACKWARD)

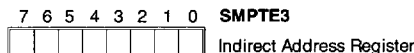
VLOCK - This is a hardware driven bit which indicates that genlock has been achieved with the selected video SYNC source.

FRAME & FIELD - The hardware SYNC separator detects the field and frame from the selected video input. The even/odd fields are identified by a 1/0 in bit 6. Bit 7, FRAME, is valid for PAL video after line 6. Bit 6, FIELD, is valid after line 5 in NTSC mode or line 2 in PAL mode.

The SMPTE2 register is the register which points to the 57 indirect registers. When reading or writing an indirect register, the value in the ADDRESS pointer, SMPTE2 bits 5 to 0, is the address of the register accessed through SMPTE3. If the AUTOINC bit is set to one, at the end of an access cycle to SMPTE3, ADDRESS will automatically increment. Otherwise, ADDRESS holds its value.



SMPTE3 is the data register through which all of the indirect registers are accessed. The address for a given register must first be set in SMPTE2 before accessing that register.





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Indirect Registers

The following describes the functions controlled by the indirect registers. A map of the indirect registers follows this section.

LTC Read Registers IR0-IR7 (read-only)

These read only registers contain the LTC data as received. Both forward and backward frames are stored with LTC bit 0 in the LSB of IR0 and LTC bit 63 in the MSB of IR 7.

LTC Write Registers IR8-IRf

These registers contain the data to be sent by the LTC transmitter. The LSB of IR 8 is sent as LTC bit 0, and the MSB of IRf is sent as LTC bit 63. The data is transmitted as it is stored in IR8-IRf.

VITC Read 1 Registers IR10-IR17 (read-only)

These read only registers contain the VITC data as received from the video line selected in IR30. The frame is stored with VITC bit 2 in the LSB of IR 10 and VITC bit 80 in the MSB of IR 17. Note that a binary 10 sync pattern precedes every eight data bits of the VITC frame. The 10 sync pattern is not stored. The CRC is checked by the VITC receiver, and the result is reported in IR30.

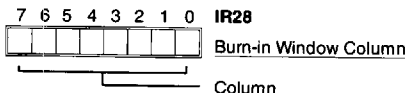
VITC Read 2 Registers IR18-IR1f (read-only)

As with the VITC Read 1 registers, these read only registers contain the VITC data as received from the video line selected in IR31. The frame is stored with VITC bit 2 in the LSB of IR 18 and VITC bit 80 in the MSB of IR 1f. The result of the CRC check is reported in IR31.

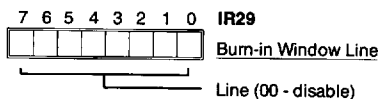
VITC Write Registers IR20-IR27

These registers contain the data to be output by the VITC generator. The VITC frame is output with the LSB if IR20 in VITC bit 2 and the MSB of IR27 in VITC bit 80. Note that the binary 10 sync pattern which precedes every eight data bits of the VITC frame is automatically generated by the VITC generator. The CRC is also automatically generated by the VITC generator.

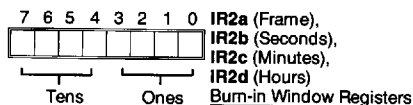
The next two registers control the position of the SMPTE video display, burn-in, window within the video raster. The window size is about one third the width of the screen and 32 lines high. IR28 selects the video column in which the burn-in window starts.



IR29 selects the video line which starts the SMPTE video display window in the video output. When this register is set to 0, there will be no Burn-In Window displayed in the video output.

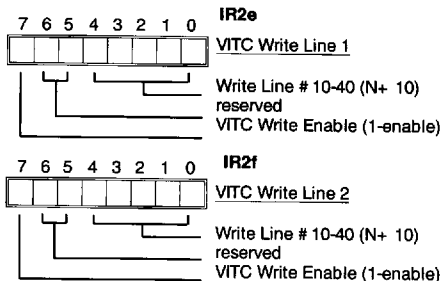


These registers contain the character codes used for the SMPTE time code in the burn-in window which overlays the source in the video output. An internal character generator converts the BCD nibbles to display characters.



CODE	CHARACTER	CODE	CHARACTER
0	0	8	8
1	1	9	9
2	2	A	Do Not Use
3	3	B	?
4	4	C	□
5	5	D	■
6	6	E	
7	7	F	Blank

VITC code is normally output on two separate video lines in each field for redundancy. These two registers allow the individual line selection and output enables for the two VITC lines.

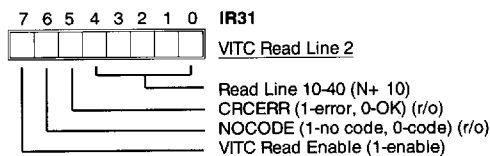
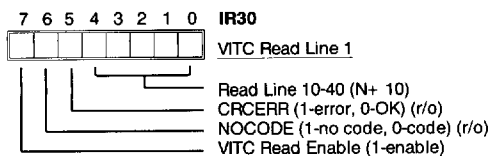


Write Line - Selects the video line on which the VITC code will be output. The video line on which the code is output will be the number in this register plus 10; e.g. writing a 1 to this register will cause the code to be output on line 11.

VITC Write Enable - Enables the output of VITC code on the specified line.



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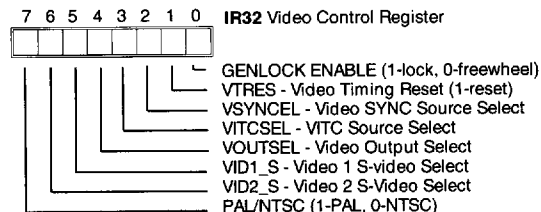


As with the VITC Write Line Register, these registers allow control of the individual redundant VITC read lines. The processor can also reprogram these dynamically to allow for scanning of VITC code when the source lines are unknown.

Read Line - Selects the line from which VITC code is to be read within each field. It works identically to the Write Line in that the video line selected is the number in this register plus 10.

CRCERR - This bit is reset to zero when a valid VITC code has been received. It is valid from the end of the selected video line until the end of the selected line in the next field.

NOCODE - This bit is set when a framing error occurs in the VITC code, i.e. not all the bits of the code were received by the time the end of the video line occurred. Both CRCOK and NOCODE must be zero to qualify a VITC code.



GENLOCK ENABLE - When set, this bit enables the genlock circuits to sync to the selected video input signal. When reset to 0, the video sync will "freewheel," generating video timing from the internal oscillator. The freewheel mode would be selected when striping LTC to allow synchronization with a MIDI sequencer or other strictly timed audio source.

VTRES - When set, this bit clears the video timing counters to dot zero of line 1 of field 1. This is useful when the video is free running, not genlocked and LTC sync needs to be synchronized to an event such as the CLICK input.

VSYNSEL - When set to 1, this bit selects the video input source from Video 2 (Y2) to be the SYNC source for the internal video timing. Otherwise, when reset to 0, Video 1 (Y1) is selected.

VITCSEL - When set to 1, this bit selects the video input source from Video 2 (Y2) to be the VITC time code source for the VITC receiver. Otherwise, when reset to 0, Video 1 (Y1) is selected.

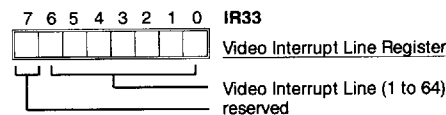
VOUTSEL - When set to 1, this bit selects the video input source from Video 2 (Y2, C2) to be output on the video outputs (YOUT, COUT). When reset to 0 Video 1 (Y1, C1) are selected.

VID1_S - When set to 1, this bit causes the Video 1 source to be treated as S-Video. Otherwise, when cleared to 0, the Video 1 source is treated as composite video.

VID2_S - When set to 1, this bit causes the video 2 source to be treated as S-Video. Otherwise, when cleared to 0, the Video 2 source is treated as composite video.

PAL/NTSC - When set to 1, this bit causes the video to be synchronized with PAL timing. Otherwise, when cleared to 0, video is synchronized with NTSC timing.

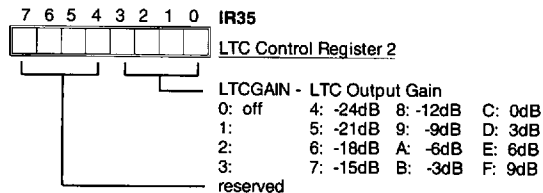
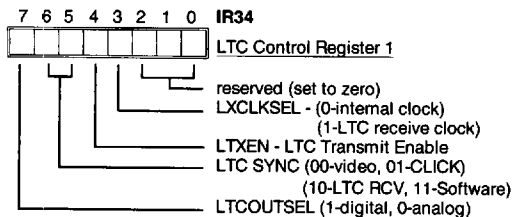
Video Interrupt Line - This register selects the video line after which the Video Line Interrupt will occur. The actual video line number is the number in the register plus one.





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LXCLKSEL - This bit controls the source for the LTC transmit clock divider input. A 0 selects the internal 14.318MHz clock and a 1 selects the LTC receive clock. When the LTC receive clock is selected as the source to the LTC transmit clock divider, the clock rate is first doubled before being input to the divider so that loading a divider value of 001 will result in the LTC transmit clock running at the exact same rate as the LTC receive clock.

LTXEN - This bit, when set to 1, enables output of LTC code on the LTCOUT output pin. LTXEN is synchronized with the selected LTC SYNC source to ensure that only complete LTC frames are transmitted. The data to be sent by the LTC transmitter should be loaded into the associated RAM buffer before the LTCEN bit is set.

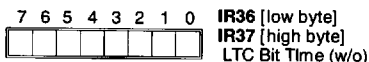
LTC SYNC - These bits select the LTC transmit sync source. Values 00, 01, 10 and 11 select start of video line 5, rising edge of CLICK, LTC receive sync pattern detect and write to IR3f respectively as the sync event. Care should be taken to disable LTXEN before changing the LTC SYNC select. Otherwise, an erroneous sync may be generated.

LTCOUTSEL - This bit, when set to 1, causes the LTCOUT pin to be a digital output. When cleared to 0, the LTCOUT pin is an analog output with gain control.

LTCGAIN - This bit sets the signal gain on the LTC audio output. The output gain is selectable in 3dB increments from -24dB to + 9dB referenced to 0VU = -10dBV. When this register is set to 0, there is no LTC audio output.

These next two write only registers control the LTC transmit bit rate. The transmit clock generator is a 12-bit divider. The upper four bits of IR37 are not used. Each bit requires two clocks. Therefore, the LTC transmit bit rate is the input clock divided by the divider value + 1, then divided by two. Since there are 80 bit times for each LTC frame, the LTC frame rate is the bit rate divided by 80.

$$\begin{aligned} \text{LTC Tx Clock} &= \text{Clock}/(\text{Divider Value} + 1) \\ \text{LTC Bit Rate} &= \text{LTC Tx Clock}/2 \\ \text{LTC Frame Rate} &= \text{LTC Bit Rate}/80 \end{aligned}$$



IR3f is not a register at all. It is simply an address which, when written and the LTC SYNC select is set for Soft SYNC, generates LTC SYNC for the LTC transmitter.





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Indirect Register Map

		7	6	5	4	3	2	1	0	
LTC	00	BINARY GROUP 1				FRAME UNITS				
	Read	01	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
		02	BINARY GROUP 3				SECONDS UNITS			
	03	BINARY GROUP 4				PHASE CORR	SECONDS TENS			
	04	BINARY GROUP 5				MINUTES UNITS				
	05	BINARY GROUP 6				BG FLAG 55	MINUTES TENS			
	06	BINARY GROUP 7				HOURS UNITS				
	07	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS		
LTC	08	SAME BIT DEFINITION AS LTC READ BUFFER								
Write	...									
OF										
VITC	10	BINARY GROUP 1				FRAME UNITS				
	READ1	11	BINARY GROUP 2				COLR FRAME	DROP FRAME	FRAMES TENS	
		12	BINARY GROUP 3				SECONDS UNITS			
	13	BINARY GROUP 4				FIELD MARK	SECONDS TENS			
	14	BINARY GROUP 5				MINUTES UNITS				
	15	BINARY GROUP 6				BG FLAG 55	MINUTES TENS			
	16	BINARY GROUP 7				HOURS UNITS				
	17	BINARY GROUP 8				BG FLAG 75	UNASSIGNED	HOURS TENS		
VITC	18	SAME BIT DEFINITION AS VITC READ1 BUFFER								
Read2	...									
1F										
VITC	20	SAME BIT DEFINITION AS VITC READ1 BUFFER								
	Write	...								
27										
Regs	28	----- BURN-IN WINDOW COLUMN -----								
	29	----- BURN-IN WINDOW LINE -----								
	2A	FRAMES -----								
	2B	SECONDS -----								
	2C	MINUTES -----								
	2D	HOURS -----								
	2E	VITC1WE	0	0	-----	VITC WRITE LINE 1				-----
	2F	VITC2WE	0	0	-----	VITC WRITE LINE 2				-----
	30	VITC1RE	NOCODE1	CRCERR1	-----	VITC WRITE LINE 1				-----
	31	VITC2RE	NOCODE2	CRCERR2	-----	VITC READ LINE 2				-----
	32	PAL	VID2_S	VID1_S	VOUTSEL	VITCSEL	VSYNCSEL	VTRES	GEN_EN	
	33	0	0	-----	VIDEO LINE INTERRUPT (LINE#)				-----	
	34	LTCOUTSEL	-----	LTCYNSCSEL	-----	LTXEN	LXCLKSEL	0	0	0
	35	0	0	0	-----	----- LTC GAIN -----				-----
	36	----- FRAME RATE (low byte, write only) -----								
37	0	0	0	0	----- FRAME RATE (high byte, write only) -----					
38	reserved									
39	reserved									
3A	reserved									
3B	reserved									
3C	reserved									
3D	reserved									
3E	reserved									
3F	----- SOFT LTC SYNC (write only, no data) -----									



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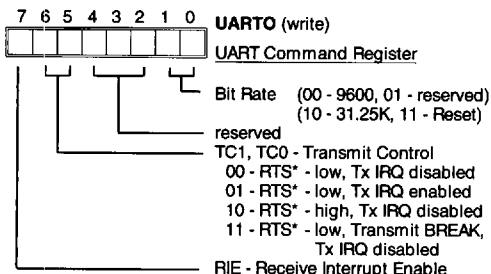
UART Registers

The UART emulates a 6850. Since the UART is tailored to MIDI applications, some of the generic 6850 functions have been omitted. The registers described below reflect that.

The two UART registers, Command/Status and Data, are accessible to the processor as shown in the following map.

UARTCS*	A1	A0	REGISTER
0	X	0	UART Command/Status Register
0	X	1	UART Data Register

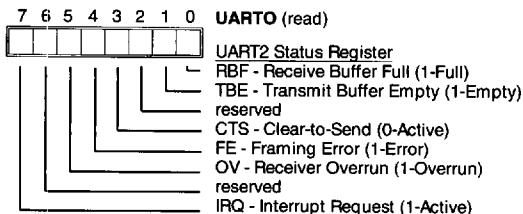
UART Command/Status Register



Bit Rate - This field selects the bit rate for data transmit and receive. After a master reset, its value is 11. One of the three bit rates must be selected in order to start the UART's operation. Writing a 11 will reset the UART.

TC1,TC0 - Bits 6 and 5, Transmit Control, provide control for transmit interrupt (when TBE is true), RTS control, and transmit BREAK level.

RIE - Bit 7, Receive interrupt enable, when set to one, enables the UART to interrupt the processor when the receive buffer is full or a receive overrun has occurred.



RBF - Bit 0, Receive Buffer Full, is set to 1 when read data is available in the UART data register. It is cleared to 0 when the UART data register is read.

TBE - Bit 1, Transmit Buffer Empty, is cleared to 0 when data is written to the UART data register. It is set to 1 when the UART transfers that data to its output shift register.

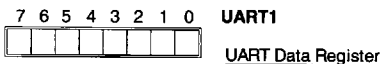
CTS - Bit 3, Clear-to-Send, is an active low status bit indicating the state of the CTS* input pin. A 0 in this bit position indicates that the modem or receiving device is ready to receive characters. A 1 indicates not ready. When CTS is inactive, 1, TBE is held at 0, the not-empty state.

FE - Bit 4, Framing Error, when set to 1, indicates that the receive character was improperly framed by the start and stop bits. It is detected by the absence of the first stop bit. This indicator is valid as long as the character data is valid.

OV - Bit 5, Receiver Overrun, is an error flag indicating that one or more characters in the data stream has been lost. It is set to 1 when a new character overwrites an old character which has not been read. The overrun error is cleared to 0 when a character is read from the UART data register.

IRQ - Bit 7, Interrupt Request, is a status bit which reflects the state of the interrupt request from the UART to the processor. When IRQ is 1, an interrupt is pending. Otherwise, no interrupt is pending.

The UART data register is actually two registers, a transmit buffer and a receive buffer. Writing to the data register causes the transmit buffer to be written. Reading from the data register causes the receive buffer to be read.





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Absolute Maximum Ratings

Operating Temperature	0 °C to + 70 °C
Storage Temperature	-65 °C to + 150 °C
Voltage on any pin to GND	-0.5V to V _{DD} + 0.5V
Voltage on V _{DD} to GND	-0.5V to + 7.0V
Power Dissipation	1.0 watt

Note: Stress above that listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Operating the device at these levels is not recommended, and specifications are not implied.

DC Characteristics $T_A = 0\text{ }^{\circ}\text{C to } + 70\text{ }^{\circ}\text{C}; V_{DD} = 5V \pm 10\%; GND = 0V$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Inputs					
Input Low Voltage	V _{IL}	-0.5		0.8	V
Input High Voltage	V _{IH}	2.0		V _{DD} + 0.5	V
Input Leakage Current	I _{LI}			10	uA
Input Capacitance	C _{IN}			7	pF
Digital Outputs					
Output Low Voltage (I _{OL} = 4.0mA)	V _{OL}			0.4	V
Output High Voltage (I _{OH} = 0.4mA)	V _{OH}	2.4			V
Tri-State Current	I _{OZ}			10	uA
Output Capacitance				10	pF
Bi-Directional Capacitance				10	pF
Analog Inputs					
Video Input Voltage (Y1, Y2, C1, C2)			1.0		V _{p-p}
LTC Differential Input Voltage		0.1			V _{p-p}
LTCIN+ , LTCIN-, CLICK, FRAME input voltage		-0.3		V _{DD} + 0.3	V
CLICK and FRAME bias voltage			V _{DD} /3		V
Analog Outputs					
Video output Voltage (YOUT, COUT)			1.0		V _{p-p}
LTC Output Voltage (Volume set at max.; I _{out} = 35mA)			2.0		V _{p-p}
LTC Output Voltage Amplitude Control Step			3		dB
LTC Output Voltage Amplitude Range			33		dB
Analog V _{DD} Supply Current	I _{DD1}			50	mA
Digital V _{DD} Supply Current	I _{DD2}			5	mA

AC Characteristics $T_A = 0\text{ }^{\circ}\text{C to } + 70\text{ }^{\circ}\text{C}; V_{DD} = 5V \pm 10\%; GND = 0V$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address setup to IOR* or IOW* command	tACS	20			ns
Address hold from IOR* or IOW* command	tAH	10			ns
Read pulse width	tRD	50			ns
Access time	tACC			150	ns
Output enable access time	tOE			50	ns
Data hold from IOR* high	tRDH	10			ns
Read command inactive time	tRHRL	210			ns
Write pulse width	tWR	50			ns
Write data setup to IOW* high	tWDS	20			ns
Write data hold from IOW* high	tWDH	10			ns
Write command inactive time	tWHWL	210			ns
CS* inactive time (Note 1)	tCHCL	20			ns
UART Port Bit Rate (Command Register [1:0]= 00)			9.6		kHz
(Command Register [1:0]= 01)			31.3		kHz
(Command Register [1:0]= 10)			reserved		kHz

Note 1: This timing parameter must be met for proper operation of indirect register access using auto-increment.



ICS2008

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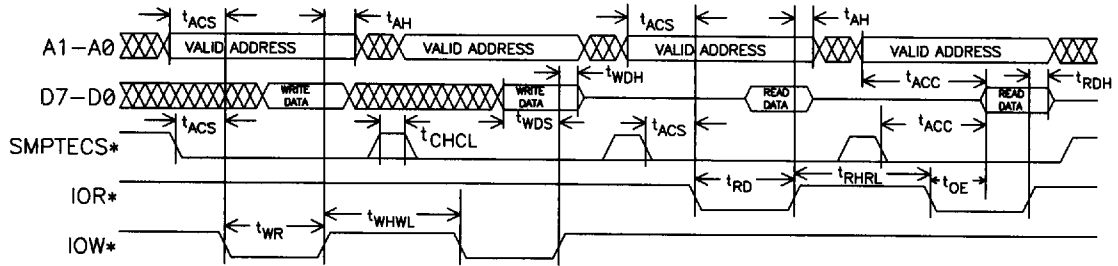


Figure 3 - Host Processor Bus Timing



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Applications

Crystal Oscillator

This oscillator will operate properly with either a serial or parallel resonant crystal. If frequency accuracy is critical, a parallel resonant crystal is recommended. In this case the load capacitance is the series equivalent of the two capacitors connected

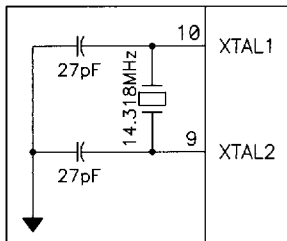


Figure 4 - Crystal Oscillator

from the crystal to ground.

Typical capacitance values of 27pF will produce a loading capacitance of about 15pF (with stray capacitance figured in).

Threshold Bypass Inputs

These inputs are used to set the clamping, SYNC extraction and data extraction threshold voltages. The values shown in Figure 5 are selected for a nominal RS-170 signal of 1Vp-p.

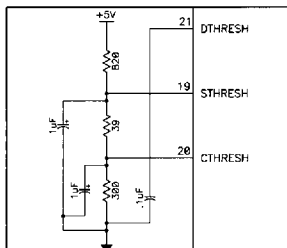


Figure 5 - Threshold Bias

If there are problems locking the ICS2008 to incoming video, check the video on Y1 or Y2 with respect to CTHRESH and STHRESH.

CTHRESH is the threshold to which the input video sync tips are clamped. The CTHRESH level is nominally 1.3V. With the incoming video riding on this 1.3V DC level, the internal SYNC separator sizes the video at 20 IRE up from the SYNC tips. This level, STHRESH, is nominally 1.44V. The SYNC separator ignores short pulses which fall below the STHRESH level such as these that come from the chroma component of the video.

Care should be taken to keep lead to these pins short and clear of any digital signal traces.

Video Inputs

Y1, Y2, C1 and C2 pins must be capacitively coupled to the terminated video source(s). These inputs are clamped to the CTHRESH level. A typical coupling capacitance is .1uF.

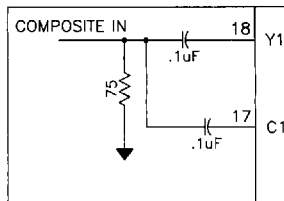


Figure 6 - Composite Input

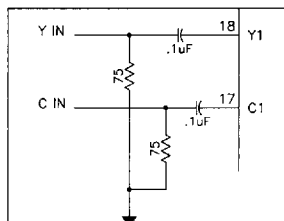


Figure 7 - S-Video Input

Video Outputs

YOUT and COUT are outputs of analog multiplexers which select the video source from Y1, C1 or Y2, C2. These outputs are not buffered. This minimizes signal distortion. It is, therefore, important to keep the capacitive and resistive load on the YOUT and COUT

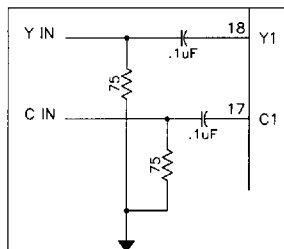


Figure 8 - Video Output

pins to a minimum. A video output buffer is shown in Figure 8. The plus input of the opamp should be high impedance, and its output should be able to drive a 75 ohm load with an appropriate video bandwidth. In general, composite NTSC and S-video signals have a bandwidth of 4.2MHz. A minimum output buffer bandwidth of 10MHz is recommended. Care should be taken in board layout to minimize stray capacitance on the YOUT and COUT pins. Otherwise, there could be high frequency rolloff. This could result in a loss of chrominance amplitude.



ICS2008

A

Self Biased Inputs

The CLICK and FRAME inputs are biased to $1/2 V_{DD}$ and connected to plus inputs of two comparators. The minus inputs are internally biased to $1/2 V_{DD}$. When CLICK or FRAME sources are analog, they should be capacitively coupled to the input pin. However, if the sources are digital, they may be tied to the pins directly. It is important to make sure that the digital levels into these pins swing above and below the $1/2 V_{DD}$ threshold of the comparators. This is not a problem with digital CMOS sources, but it could be with TTL sources.

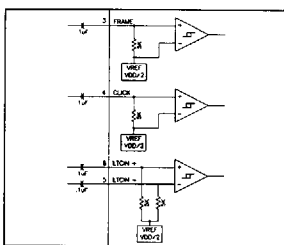


Figure 9 - Self Biased Inputs

LTCIN+ and LTCIN- are comparator inputs for the LTC input. This differential input is provided to maximize noise immunity. If the LTC source is single ended, the LTCIN- should be capacitively coupled to the ground reference of that source. If the LTC source is digital, set the LTCIN- to the desired threshold, and connect the digital source to LTCIN+.

LFC Pin

This pin should be tied to V_{DD} .

Programming

The ICS2008 is a SMPTE time code input/output device with a UART which can be used as a MIDI UART or transport control UART. All of the time critical functions to read and generate time code are performed by the chip's hardware, but all of the intelligence for processing time codes and generating the time code values are performed via an external processor. This makes the ICS2008 flexible enough for a broad range of applications without making the processing requirements on the host system too great.

In the case of the LTC receiver, LTC data is received into a temporary buffer and transferred into the LTC read register (IR0 to IR7) when the last bit of LTC data has been received. It should be noted that the data is transferred before the SYNC pattern has been received. Once the data is in the LTC receive buffer, the LRI bit is set to one in the SMPTE0 register. If the LRIEN bit (SMPTE0) is set to a one, an interrupt will be generated. The interrupt is cleared when the SMPTE0 register is read. The data in the LTC receive buffer remains valid until the next LTC frame has been completely received.

The LTC generator transfers data from the LTC Write registers (IR8 to IRf) to the output buffer when the LTC generator is enabled; LTCEN is set to one. Data transfers for subsequent LTC frames occur eight bit times before the end of the LTC frame being output. Remember that a LTC frame ends with a 16 bit SYNC pattern. The LXI interrupt bit in SMPTE0 is set to one when LTC Write register data is transferred to the output buffer.

The UART has a four deep FIFO for its receive buffer. This allows for relaxed interrupt latency requirements. In the case of MIDI bit rates, the receiver will not overflow even if the interrupt response delay is 1msec.



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Indirect Register Access

Indirect registers are accessed via the SMPTE2 (address) and SMPTE3 (data) registers. To read an indirect register, the program must first write its address to SMPTE2. Then the data is read from SMPTE3. Writing to an indirect register is similar. First, the address is written to SMPTE2. Then the data is written to SMPTE3.

In order to minimize the number of accesses required to read or write a block of registers, an auto-increment function is provided. If the MSB of SMPTE2 is written to a one with the address, the address is incremented after each read or write access to SMPTE3. For example, if one wants to read the LTC Read registers, IR0 to IR7, SMPTE2 is written to a 80h. Then SMPTE3 is read eight times. The first byte read is from IR0 followed by IR1, etc. The auto increment feature will not operate properly if CS* is not returned to the inactive state between accesses. See the AC timing section.

Interrupt Processing

Interrupts can be generated from four sources, LTC receiver, LTC generator, video line count and UART. The interrupt status of the first three interrupts, LRI, LXI, and VLI are in the SMPTE0 register. After this register is read, all three interrupts are cleared. It is, therefore, necessary to save the state of the interrupt status and process all active interrupts.

The UART interrupt status is in the UART0 register. The receive interrupt is cleared by reading the receive data register, UART1. The transmit interrupt is cleared by writing data to the transmit data register, UART1.

Reading LTC

LTC input data is available in the LTC Read registers after the last LTC data bit has been received. It is not necessary to wait for the LTC SYNC pattern to be complete. When LTC read data is available the LRI bit in SMPTE0 is set to one. If LRIEN is set to one, an interrupt is generated. LRI and the interrupt are cleared by reading SMPTE0. Data will remain valid until the last LTC data bit of the next frame has been received.

Generating LTC

A typical program for generating LTC output would first setup the LTC control registers and the LTC bit time registers. Then time code data would be written to the LTC Write register. Once this setup is done the LTC output would be enabled by setting LTCEN to a one. LTC output starts when a LTC SYNC is received. The LTC SYNC source is selected as part of the setup. While the LTC generator is waiting for SYNC, the data in the LTC Write register is transferred to the output buffer. When the transfer is complete the LXI status bit is set to a one. The data for the next LTC output frame can then be loaded. The LXI status bit will be set to a one after the data transfer at the end of the first LTC output frame. At this point the LTC Write register is ready to receive data for the third LTC output frame.

The SMPTE1 register contains two status bits which indicate whether LTC data is being received and if so which direction. LTCLOCK is set to one when the LTC receiver has received a valid LTC SYNC pattern and data is still coming in. CODEDIR indicates the direction of the LTC SYNC pattern. This is useful to tell whether a tape with LTC is shuttling forwards or backwards.

Reading VITC

To read VITC code one must first setup IR30 thru IR33. The VITC Read Line registers, IR30 and IR31, select the video line from which VITC code is to be read. The MSB is the enable for VITC reading. The Read Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 15 is desired, a 5 should be programmed in the Read Line field. IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

The VLOCK bit in the SMPTE1 register indicates whether the ICS2008 is genlocked to the selected video source. Without the VLOCK status set to one, no VITC read will occur.

With VLOCK set to one and the control registers properly initialized VITC data is received a byte at a time from the video signal and written to the VITC Read registers. At the end of the VITC data frame the CRC byte is checked, and the result reported in bit 5 of IR30 and IR31. In addition to the CRC check, if a full VITC data frame is not received, the NOCODE bit, bit 6, is set to a one.



Generating VITC

Like reading VITC, IR2e, IR2f, IR32 and IR33 must be setup in order to generate VITC. The VITC Write Line registers, IR2e and IR2f, select the video line to which VITC code is to be written. The MSB is the enable for VITC generation. The Write Line field, bits 4 to 0, should be programmed with the desired line number minus ten. So, if line 12 is desired, a 2 should be programmed in the Write Line field. IR32 selects the source and type of video. The GENLOCK ENABLE bit must be set to a one, and the VTRES bit must be set to a zero. The Video Interrupt Line register, IR33 should be set to a line after all VITC read and write lines. This allows all of the VITC receive and generate operations to be complete before processing VITC.

With the VITC generator setup properly, when the selected video line starts, the VITC data in the VITC Write buffer, IR20 to IR27, is output. The video line interrupt, VLI in SMPTE0, is provided to allow ample processing time for VITC generation.

Burn-in Window

The burn-in window can be placed anywhere on the video display. The position of the upper left corner of the window is selected by the values written in IR28 and IR29. IR28 controls the horizontal position. Values from 00h to 71h put the corner in the first half of a video line (starting from the falling edge of HSYNC). Values from 80h to f1h put the corner in the second half of a video line. Any other values will not display the window. Care should be taken not to choose values which put the window in any part of the blanking area. IR29 controls the vertical position. The value written here is the video line number divided by 2.

IR2a to IR2d, are the registers which control the characters displayed in the burn-in window.