

P4C187/P4C187L ULTRA HIGH SPEED 64K x 1 STATIC CMOS RAMS (SCRAMS)

T-46-23-05

★ FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 10/12/15/20/25 ns (Commercial)
 - 15/20/25/35 ns (Military)
- Low Power (Commercial/Military)
 - 690 mW Active for -10 (Commercial)
 - 660/770 mW Active for -12/15
 - 550/660 mW Active for -20/25/35
 - 193/220 mW Standby (TTL Input)
 - 83/110 mW Standby (CMOS Input) P4C187
 - 1.1/5.5 mW Standby (CMOS Input) P4C187L
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply
- Separate Data I/O
- Three-State Output
- TTL/CMOS Compatible Output
- Fully TTL Compatible Inputs
- Produced with PACE II Technology™
- Standard Pinout (JEDEC Approved)
 - 22-Pin 300 mil DIP
 - 24-Pin 300 mil SOJ
 - 22-Pin 290x490 mil LCC

2

★ DESCRIPTION

The P4C187/L are 65,536-bit ultra high speed static RAMs organized as 64K x 1. The CMOS memories require no clocks or refreshing and have equal access and cycle times. The RAMs operate from a single 5V±10% tolerance power supply. Data integrity is maintained for supply voltages down to 2.0V, typically drawing 10 µA.

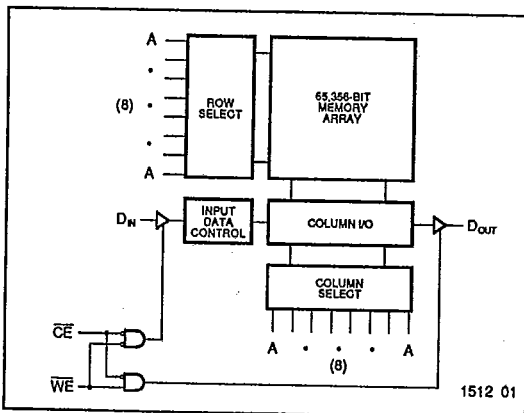
Access times as fast as 10 nanoseconds are available, greatly enhancing system speeds. CMOS reduces power consumption to a low 690 mW active, 193/83 mW standby for TTL/CMOS inputs and only 1.1 mW standby for the P4C187L. The P4C187/L are members of a family of PACE RAM™ products offering super fast access times never before available in TTL-compatible CMOS technologies.

The P4C187/L are manufactured with PACE II Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths to give 400 picoseconds loaded* internal gate delays. PACE II Technology includes two level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

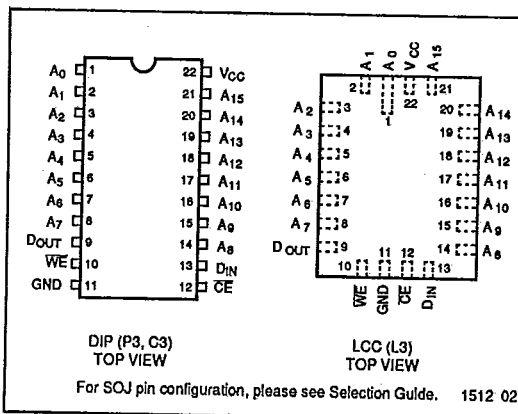
The P4C187/L are available in 22-pin 300 mil DIP, 24-pin 300 mil SOJ, and 22-pin LCC packages providing excellent board level densities.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

★ FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PERFORMANCE
SEMICONDUCTOR CORPORATION

T-46-23-05

MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC}+0.5$	V
T_A	Operating Temperature	-55 to +125	°C

1512 Tbl 01

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1512 Tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Military	-55 to +125°C	0V	5.0V ± 10%

1512 Tbl 03

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

1512 Tbl 04

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C187		P4C187L		Unit
			Min	Max	Min	Max	
V_{IH}	Input High Voltage		2.2	$V_{CC}+0.5$	2.2	$V_{CC}+0.5$	V
V_{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	-0.5 ⁽³⁾	0.8	V
V_{HC}	CMOS Input High Voltage		$V_{CC}-0.2$	$V_{CC}+0.5$	$V_{CC}-0.2$	$V_{CC}+0.5$	V
V_{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	-0.5 ⁽³⁾	0.2	V
V_{CD}	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	$I_{OL} = +10 \text{ mA}, V_{CC} = \text{Min.}$ $I_{OL} = +8 \text{ mA}, V_{CC} = \text{Min.}$		0.5 0.4		0.5 0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	$I_{OLC} = +100 \mu\text{A}, V_{CC} = \text{Min.}$		0.2		0.2	V
V_{OH}	Output High Voltage (TTL Load)	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4		2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	$I_{OHC} = -100 \mu\text{A}, V_{CC} = \text{Min.}$	$V_{CC}-0.2$		$V_{CC}-0.2$		V
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$	Mil. -10 -5	+10 +5	-5 -2	+5 +2	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CE} = V_{IH}$ $V_{OUT} = \text{GND to } V_{CC}$	Mil. -10 -5	+10 +5	-5 -2	+5 +2	μA

1512 Tbl 05

CAPACITANCES⁽⁴⁾ $(V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}, f = 1.0\text{MHz})$

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	5	pF

1512 Tbl 06

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	7	pF

1512 Tbl 07

Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

T-46-23-05

Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C187		P4C187L		Unit
			Min	Max	Min	Max	
I_{CC}	Dynamic Operating Current – 10	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open Mil. Com'l.	—	n/a 125	—	n/a n/a	mA
I_{CC}	Dynamic Operating Current – 12, 15	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open Mil. Com'l.	—	140 120	—	140 120	mA
I_{CC}	Dynamic Operating Current – 20, 25, 35	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open Mil. Com'l.	—	120 100	—	120 100	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ $V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open Mil. Com'l.	—	40 35	—	40 35	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$ $V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ Mil. Com'l.	—	20 15	—	1.0 0.2	mA

n/a = Not Applicable

1512 Tbl 08

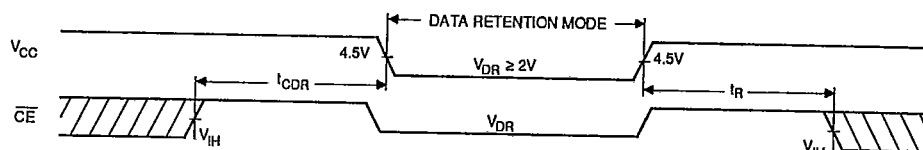
DATA RETENTION CHARACTERISTICS (P4C187L Only)

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	Mil. Com'l.		10 10	15 15	600 150	900 225	μA μA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0					ns
$t_R^\dagger$	Operation Recovery Time		t_{RC}^s					ns

* $T_A = +25^\circ\text{C}$ $s_{t_{RC}}$ = Read Cycle Time † This parameter is guaranteed but not tested.

1512 Tbl 09

DATA RETENTION WAVEFORM



1512 03



AC CHARACTERISTICS—READ CYCLE

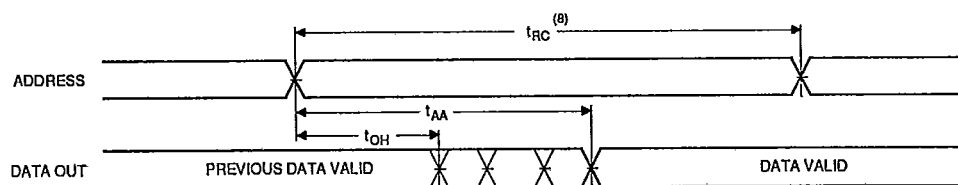
T-46-23-05

(V_{CC} = 5V ± 10%, All Temperature Ranges)⁽²⁾

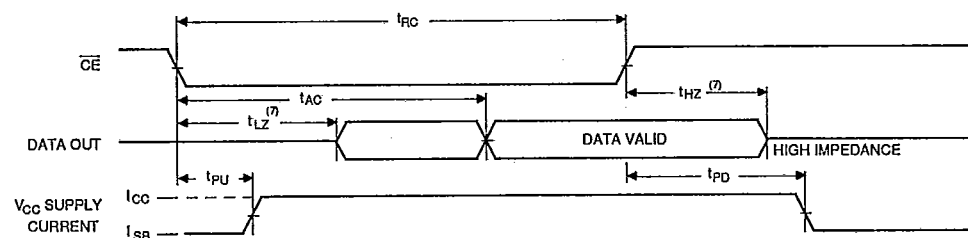
Symbol	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{RC}	Read Cycle Time	10		12		15		20		25		35		ns
t _{AA}	Address Access Time		10		12		15		20		25		35	ns
t _{AC}	Chip Enable Access Time		10		12		15		20		25		35	ns
t _{OH}	Output Hold from Address Change	0		0		1		2		2		3		ns
t _{LZ}	Chip Enable to Output in Low Z	0		0		0		1		2		2		ns
t _{HZ}	Chip Disable to Output in High Z		5		6		8		10		12		17	ns
t _{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t _{PD}	Chip Disable to Power Down Time		10		12		15		20		25		35	ns

*V_{CC} = 5V ± 5% for -10

1512 Tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1 ⁽⁵⁾

1512 04

TIMING WAVEFORM OF READ CYCLE NO. 2 ⁽⁶⁾

1512 05

Notes:

5. $\overline{CE}$ is low and $\overline{WE}$ is high for READ cycle.
6. $\overline{WE}$ is high, and address must be valid prior to or coincident with $\overline{CE}$ transition low.
7. Transition is measured $\pm 200\text{mV}$ from steady state voltage prior to

change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

8. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

T-46-23-05

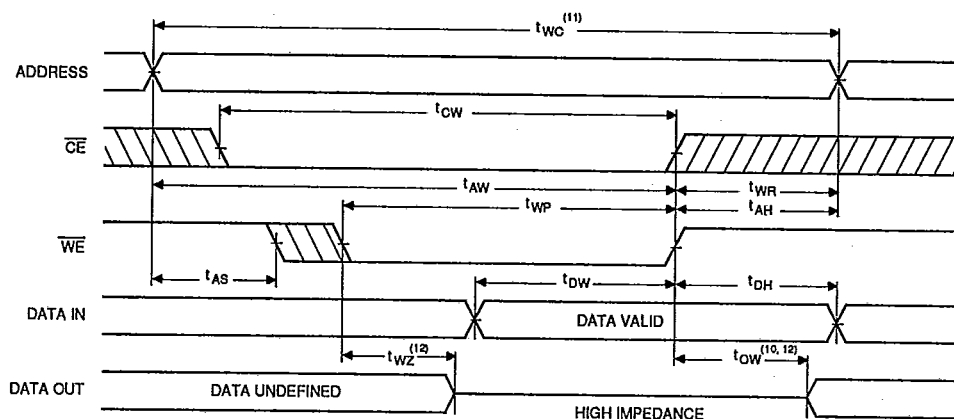
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Symbol	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		25		35		ns
t_{CW}	Chip Enable Time to End of Write	8		10		12		15		20		25		ns
t_{AW}	Address Valid to End of Write	8		10		12		15		20		25		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	8		10		12		15		20		25		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		0		0		ns
t_{WR}	Write Recovery Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		10		13		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		8		12		15		17	ns
t_{OW}	Output Active from End of Write	0		0		0		0		0		0		ns

* $V_{CC} = 5V \pm 5\%$ for -10

1512 Tbl 11

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED)⁽⁹⁾



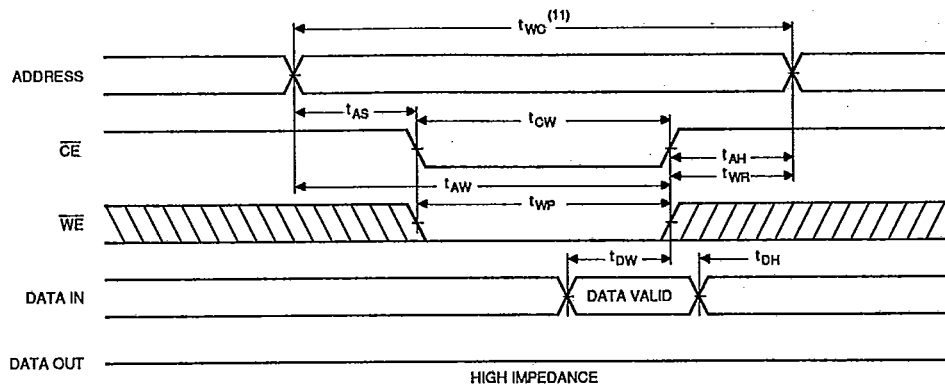
1512 06

Notes:

9. CE and WE must be low for WRITE cycle.
10. If CE goes high simultaneously with WE high, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.

12. Transition is measured $\pm 200mV$ from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) ⁽⁹⁾



1512 07

AC TEST CONDITIONS

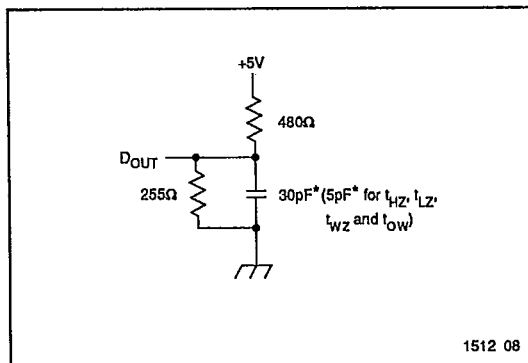
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

1512 Tbl 12

TRUTH TABLE

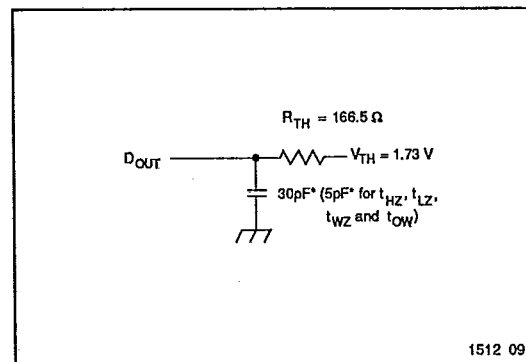
Mode	$\overline{CE}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

1512 Tbl 13



1512 08

Figure 1. Output Load



1512 09

Figure 2. Thevenin Equivalent

* including scope and test fixture.

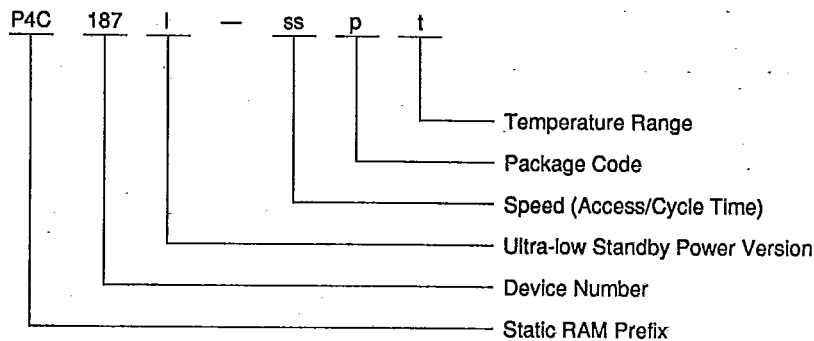
Note:

Due to the ultra-high speed of the P4C187/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between V_{CC} and ground. To

avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).

ORDERING INFORMATION

T-46-23-05



- L = Ultra-low standby power designator L, if needed.
- ss = Speed (access/cycle time in ns), e.g., 10, 15
- p = Package code, i.e., P, J, C, L.
- t = Temperature range, i.e., C, M, MB.

1512 10

PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide standard
L	Leadless Chip Carrier (ceramic)

1512 Tbl 14

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

1512 Tbl 15



T-46-23-05

SELECTION GUIDE

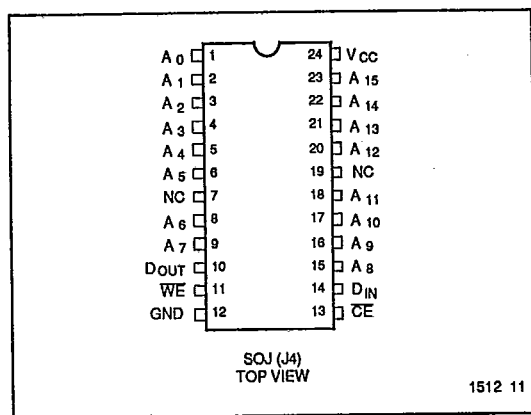
The P4C187/L are available in the following temperature, speed and package options.

Temperature Range	Package	Speed (ns)					
		10	12	15	20	25	35
Commercial	Plastic DIP	-10PC	-12PC	-15PC	-20PC	-25PC	N/A
	Plastic SOJ	-10JC	-12JC	-15JC	-20JC	-25JC	N/A
	Sidebrazed DIP	-10CC	-12CC	-15CC	-20CC	-25CC	N/A
	LCC	-10LC	-12LC	-15LC	-20LC	-25LC	N/A
Military Temp.	Sidebrazed DIP	N/A	N/A	-15CM	-20CM	-25CM	-35CM
	LCC	N/A	N/A	-15LM	-20LM	-25LM	-35LM
Military Processed*	Sidebrazed DIP	N/A	N/A	-15CMB	-20CMB	-25CMB	-35CMB
	LCC	N/A	N/A	-15LMB	-20LMB	-25LMB	-35LMB

1512 Tbl 16

* Military temperature range with MIL-STD-883 Revision C, Class B processing.
N/A = Not Available

SOJ PIN CONFIGURATION



TECHDOC 1512