P54/74PCT841A/B—P54/74PCT843A/B P54/74PCT846A/B BUS INTERFACE LATCHES

PRELIMINARY

T-46-07-27

FEATURES

- Equivalent to Am29841/843/846 Bipolar Registers
- Full CMOS Implementation
- Low Power Operation
- Fully TTL Compatible Input and Output Levels
- Buffered Common Clear and Preset Input
- High Speed Parallel Latches
- Buffered Common Latch Enable Input
- Clamp Diodes on all Inputs for Ringing Suppression
- Produced with PACE Technology™
- Compact Pinout
  - 24-Pin 300 mil DIP, SOIC
  - 28-Pad 450 mil sq. LCC

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DESCRIPTION

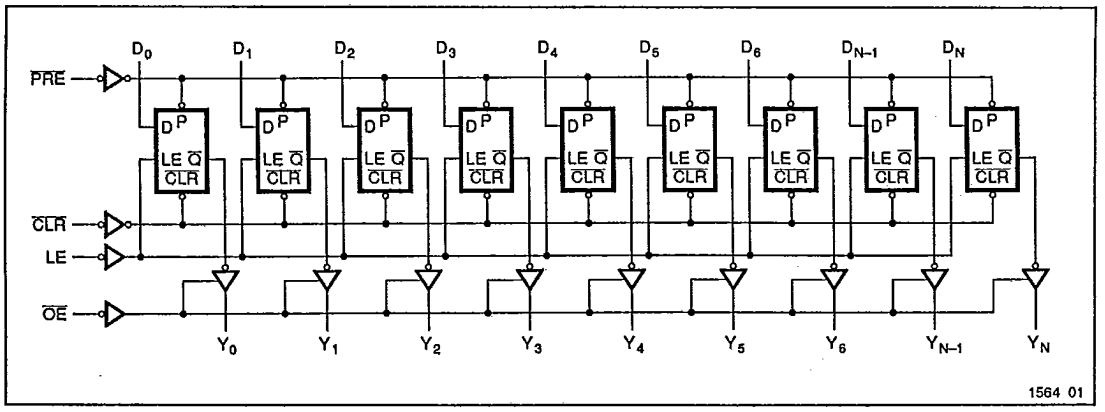
The P54/74PCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The P54/74PCT841 is a buffered 10-bit wide version of the popular 'PCT373 function. The P54/74PCT843 is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) controls making it ideal for parity bus interfacing in high-performance systems. The P54/74PCT846 is an inverting 8-bit buffered latch with all the 'PCT843 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiusers control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The P54/74PCT800 high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The P54/74PCT800 interface family is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM



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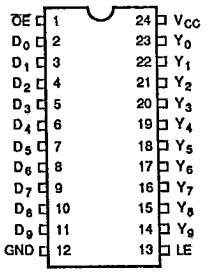
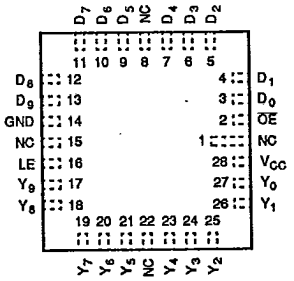
PIN CONFIGURATIONS

LOGIC SYMBOLS

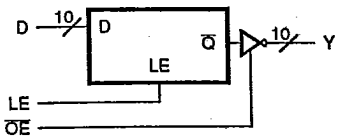
P54/74PCT841 10-BIT LATCH



DIP (D4, P4) SOIC (S4)

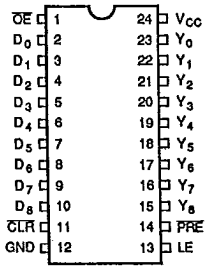


LCC (L5-1)

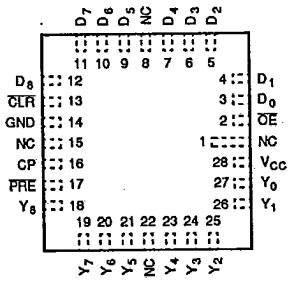


1564 02

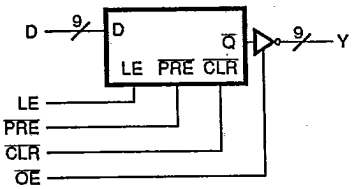
P54/74PCT843 9-BIT LATCH



DIP (D4, P4) SOIC (S4)



LCC (L5-1)



1564 03

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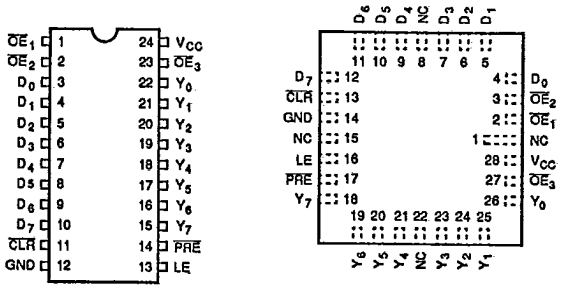
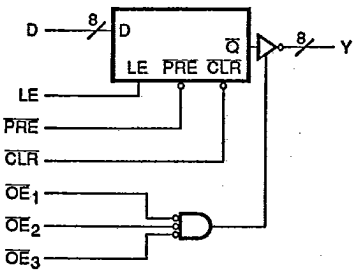
PIN CONFIGURATIONS

P54/74PCT846 8-BIT LATCH



DIP (D4, P4) SOIC (S4) LCC (L5-1)

LOGIC SYMBOL



1564 04

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PIN DESCRIPTION

Name	I/O	Description
P54/74PCT841/43 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_1	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

1564 Tbl 01

Name	I/O	Description
P54/74PCT846 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_1	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1564 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1564 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1564 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1564 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –15mA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –24mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)			0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–75			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQC}	Quiescent Power Supply Current (CMOS inputs) Com'l / Mil	.003 / .003	0.3 / 0.5	mA / mA	V_{CC} = MAX, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, f = 0, Outputs Open
I_{CCQT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open, LE = V_{CC}
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, LE = V_{CC}, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			5.0	mA	V_{CC} = MAX, LE = V_{CC}, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10mHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
			6.5[4]	mA	V_{CC} = MAX, LE = V_{CC}, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			14.5[4]	mA	V_{CC} = MAX, LE = V_{CC}, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQC} + I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CCQC} = Quiescent Current with CMOS input levels
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	P54/74PCT841A-846A				P54/74PCT841B-846B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Data (D_1) to Output (Y_1) (LE = HIGH)	C_L = 50pF R_L = 500Ω	– –	11.0[2] 11.0	– –	9.5[2] 9.5	– –	7.5[2] 7.5	– –	6.5[2] 6.5	ns ns	1 5
t_{PLH} t_{PHL}	Data (D_1) to Output (Y_1) (LE = HIGH)	C_L = 300pF[4] R_L = 500Ω	– –	15.0 15.0	– –	13.0 13.0	– –	15.0 15.0	– –	13.0 13.0	ns ns	1 5
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_1	C_L = 50pF R_L = 500Ω	– –	16.0 16.0	– –	12.0 12.0	– –	10.5 10.5	– –	8.0 8.0	ns ns	1 6
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_1	C_L = 300pF[4] R_L = 500Ω	– –	20.0 20.0	– –	16.0 16.0	– –	18.0 18.0	– –	15.5 15.5	ns ns	1 6
t_{PLH}	Propagation Delay Preset to Y_1	C_L = 50pF R_L = 500Ω	–	14.0	–	12.0	–	10.0	–	8.0	ns	1 5
t_{PHL}	Propagation Delay Clear to Y_1		–	15.0	–	13.0	–	11.0	–	10.0	ns	1 5
t_{PZH} t_{PZL}	Output Enable Time OE ↓ to Y_1		– –	15.0 15.0	– –	14.0 14.0	– –	8.5 8.5	– –	8.0 8.0	ns ns	1, 7, 8
t_{PZH} t_{PZH}	Output Enable Time OE ↓ to Y_1	C_L = 300pF[4] R_L = 500Ω	– –	25.0 25.0	– –	23.0 23.0	– –	15.0 15.0	– –	14.0 14.0	ns ns	1, 7, 8
t_{PZH} t_{PLZ}	Output Disable Time OE ↑ to Y_1	C_L = 5pF[4] R_L = 500Ω	– –	10.0 10.0	– –	9.0 9.0	– –	6.5 6.5	– –	6.0 6.0	ns ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OE ↑ to Y_1	C_L = 50pF R_L = 500Ω	– –	12.0 12.0	– –	12.0 12.0	– –	7.5 7.5	– –	7.0 7.0	ns ns	1, 7, 8
t_{PLH} t_{PHL}	DATA (D_1) to Output (Y_1) (LE = HIGH)		– –	12.0[3] 12.0	– –	10.0[3] 10.0	– –	9.0[3] 9.0	– –	8.0[3] 8.0	ns ns	1 5

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AC OPERATING REQUIREMENTS

Symbol	Parameter	Test Conditions	P54/74PCT841A-846A				P54/74PCT841B-846B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{SU}	Data to LE Set-up Time	C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns	9
t_H	Data to LE Hold Time		3.0	–	2.5	–	2.5	–	2.5	–	ns	9
t_{SU}	Preset Recovery ($\overline{PRE}$ ↑) Time		–	17.0	–	14.0	–	13.0	–	10.0	ns	9
t_{SU}	Clear Recover ($\overline{CLR}$ ↑) Time		–	17.0	–	14.0	–	10.0	–	10.0	ns	9
$t_W(H)$	LE Pulse Width HIGH		6.0	–	6.0	–	4.0	–	4.0	–	ns	5
$t_W(L)$	Preset Pulse Width LOW		9.0	–	8.0	–	4.0	–	4.0	–	ns	5
$t_W(L)$	Clear Pulse Width LOW		9.0	–	8.0	–	4.0	–	4.0	–	ns	5

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Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These limits do not apply to the P54/74PCT846.
3. Limits for P54/74PCT846.
4. This parameter is guaranteed but not tested.

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FUNCTION TABLES§
P54/74PCT841/43

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_1	O_1	Y_1	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	HighZ
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance.

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FUNCTION TABLES§
P54/74PCT841/46

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_1	O_1	Y_1	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	HighZ
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance.

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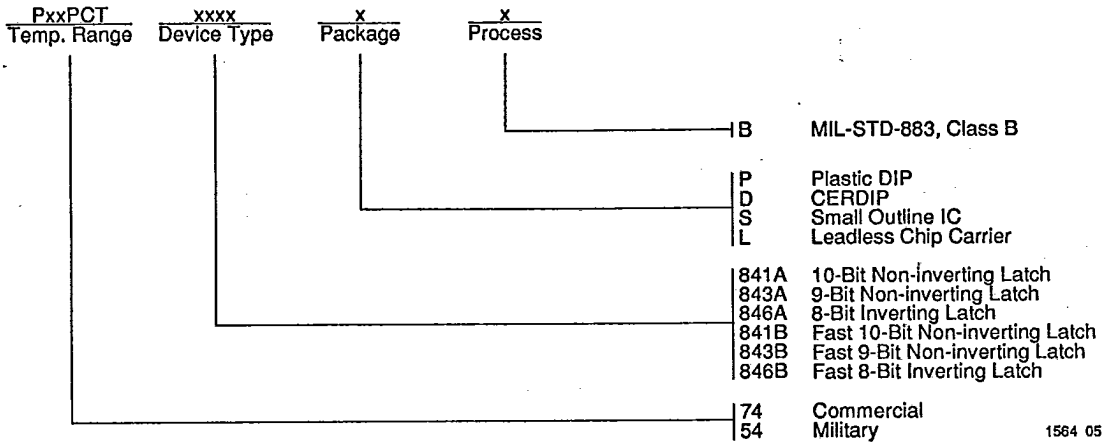
ORDERING INFORMATION



TECHDOC 1564