

# P29PCT52A/B P29PCT53A/B OCTAL REGISTERED TRANSCEIVER

PRELIMINARY  
T-52-31

## ★ FEATURES

- Equivalent to Am2952/52 In pinout and function
- Full CMOS Implementation
- Low Power Operation
- Fully TTL Compatible Input and Output Levels
- $I_{OL} = 64 \text{ mA}$  (Commercial) and  $32 \text{ mA}$  (Military)
- Produced with PACE Technology™
- Compact Pinout
  - 24-Pin 300 mil DIP, SOIC
  - 28-Pin 450 mil sq. LCC

## ★ DESCRIPTION

The P29PCT52A/B AND P29PCT53A/B have two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The P29PCT52 is an inverting option of the P29PCT53.

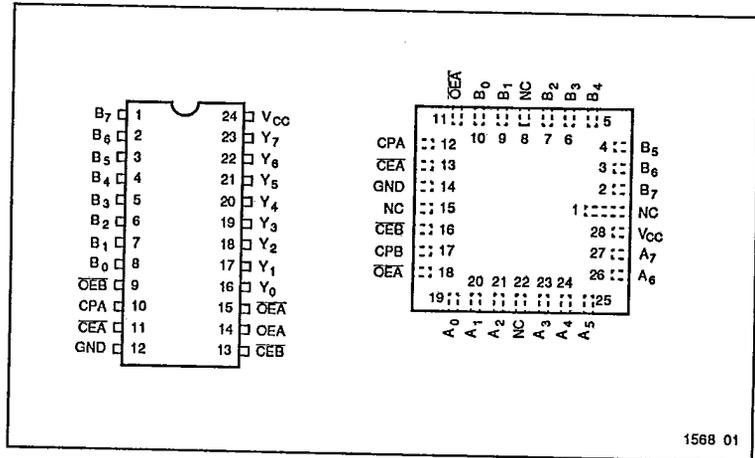
The P29PCT52 and P29PCT53 are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel

lengths resulting in 500 picoseconds loaded\* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

\* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picosecond at room temperature.



## ★ PIN CONFIGURATIONS



Means Quality, Service and Speed

★  
**REGISTERED FUNCTION TABLE**  
 (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

1568 Tbl 01

**OUTPUT CONTROL** T-52-31

$\overline{OE}$	Internal Q	Y-Outputs		Function
		52A/B	53A/B	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

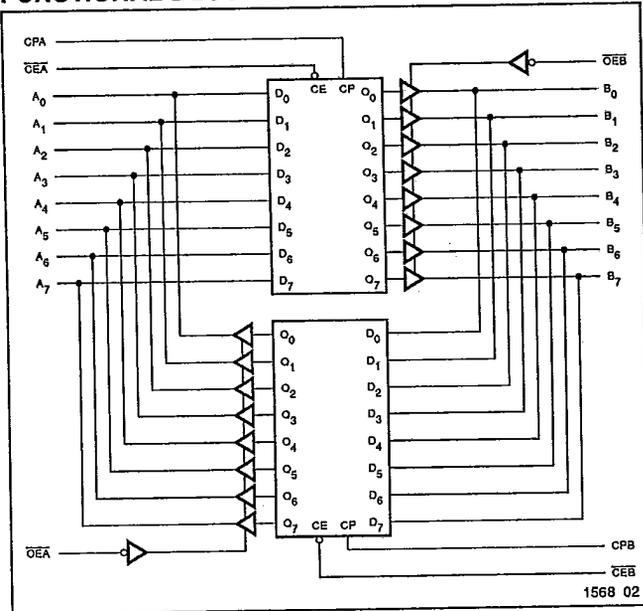
1568 Tbl 02

**PIN DESCRIPTION**

Name	I/O	Description
A <sub>0-7</sub>	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B <sub>0-7</sub>	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B <sub>0-7</sub> lines. When $\overline{OEB}$ is HIGH, the B <sub>0-7</sub> outputs are in the high impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A <sub>0-7</sub> lines. When $\overline{OEA}$ is HIGH, the A <sub>0-7</sub> outputs are in the high impedance state.

1568 Tbl 03

**FUNCTIONAL BLOCK DIAGRAM**



1568 02

**ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>**

Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>A</sub>	Ambient Temperature Under Bias	-55 to +125	°C
V <sub>CC</sub>	V <sub>CC</sub> Potential to Ground	-0.5 to +7.0	V
I <sub>IN</sub>	Input Current	-30 to +5.0	mA

Notes: 1588 Tbl 04  
 1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

**T-52-31**

Symbol	Parameter	Value	Unit
I <sub>OUTPUT</sub>	Current Applied to Output	100	mA
V <sub>IN</sub>	Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	Voltage Applied to Output	-0.5 to V <sub>CC</sub> + 0.5	V

1588 Tbl 05  
 2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

**RECOMMENDED OPERATING CONDITIONS**

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V <sub>CC</sub> )	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1588 Tbl 06

1588 Tbl 07

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions)

Symbol	Parameter	Min	Typ <sup>1</sup>	Max	Units	V <sub>CC</sub>	Conditions	
V <sub>IH</sub>	Input HIGH Voltage	2.0		V <sub>CC</sub> + 0.5	V			
V <sub>IL</sub>	Input LOW Voltage	-0.5		0.8	V			
V <sub>H</sub>	Hysteresis		.35		V		All inputs	
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	MIN	I <sub>IN</sub> = -18mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0.2V, or V <sub>CC</sub> - 0.2V		V <sub>CC</sub> - 0.2	V		I <sub>OH</sub> = -32μA	
		Military/Commercial (CMOS)		V <sub>CC</sub> - 0.2	V	MIN	I <sub>OH</sub> = -300μA	
		Military (TTL)		2.4	V	MIN	I <sub>OH</sub> = -15mA	
		Commercial (TTL)		2.7	V	MIN	I <sub>OH</sub> = -24mA	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0.2V, or V <sub>CC</sub> - 0.2V			0.2	V	I <sub>OL</sub> = 300μA	
		Military/Commercial (CMOS)			0.2	V	MIN	I <sub>OL</sub> = 300μA
		Military (TTL)			0.55	V	MIN	I <sub>OL</sub> = 48mA
		Commercial (TTL)			0.55	V	MIN	I <sub>OL</sub> = 64mA
I <sub>IH</sub>	Input HIGH Current			5	μA	MAX	V <sub>IN</sub> = V <sub>CC</sub>	
I <sub>IL</sub>	Input LOW Current			-5	μA	MAX	V <sub>IN</sub> = GND	
I <sub>IH</sub>	Input HIGH Current <sup>3</sup>			5	μA	MAX	V <sub>IN</sub> = 2.7V	
I <sub>IL</sub>	Input LOW Current <sup>3</sup>			-5	μA	MAX	V <sub>IN</sub> = 0.5V	
I <sub>IH</sub>	Input HIGH Current (I/O Pins only)			15	μA	MAX	V <sub>IN</sub> = V <sub>CC</sub>	
I <sub>IL</sub>	Input LOW Current (I/O Pins only)			-15	μA	MAX	V <sub>IN</sub> = GND	
I <sub>IH</sub>	Input HIGH Current <sup>3</sup> (I/O Pins only)			15	μA	MAX	V <sub>IN</sub> = 2.7V	
I <sub>IL</sub>	Input LOW Current <sup>3</sup> (I/O Pins only)			-15	μA	MAX	V <sub>IN</sub> = 0.5V	
I <sub>OS</sub>	Output Short Circuit Current <sup>2</sup>	-60			mA	MAX	V <sub>OUT</sub> = 0.0V	
C <sub>IN</sub>	Input Capacitance <sup>3</sup>		5	10	pF		All inputs	
C <sub>OUT</sub>	Output Capacitance <sup>3</sup>		9	12	pF		All outputs	

Notes: 1588 Tbl 08  
 1. Typical limits are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C ambient.  
 2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.  
 3. This parameter is guaranteed but not tested.



★ DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ <sup>1</sup>	Max	Units	Conditions
$I_{CCOC}$	Quiescent Power Supply Current (CMOS inputs) Com'l Mil	.003 .003	0.3 0.5	mA mA	$V_{CC} = \text{MAX}, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V, f = 0,$ Outputs Open
$I_{CCOT}$	Quiescent Power Supply Current (TTL inputs)		2.0	mA	$V_{CC} = \text{MAX}, V_{IN} = 3.4V^2,$ $f = 0,$ Outputs Open
$I_{CCD}$	Dynamic Power Supply Current <sup>3</sup>		0.25	mA/ mHz	$V_{CC} = \text{MAX},$ One Input Toggling, 50% Duty Cycle, $OE = \text{GND},$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V,$ Outputs Open
$I_{CC}$	Total Power Supply Current <sup>5</sup>		4.0	mA	$V_{CC} = \text{MAX}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz},$ $OE = \text{GND}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			6.0	mA	$V_{CC} = \text{MAX}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz},$ $OE = \text{GND}$ and $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
			7.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz},$ $OE = \text{GND}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			16.8 <sup>4</sup>	mA	$V_{CC} = \text{MAX}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz},$ $OE = \text{GND}$ and $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

1568 Tbl 09

Notes:

1. Typical values are at  $V_{CC} = 5.0V, +25^\circ\text{C}$  ambient and maximum loading.
2. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
5.  $I_{CC} = I_{CCOC} + I_{CCOT} + I_{CCD}$   
 $I_{CC} = I_{CCOC} + I_{CCOT} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CCOC}$  = Quiescent Current with CMOS input levels

$I_{CCOT}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of TTL Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_0$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_1$  = Input Frequency

$N_1$  = Number of Inputs at  $f_1$

All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

T-52-31

Sym	Parameter	P29PCT52A/53A					P29PCT52B/53B					Units	Fig. No.
		T <sub>A</sub> =+25°C V <sub>CC</sub> =+5.0V		MIL		COM'L	T <sub>A</sub> =+25°C V <sub>CC</sub> =+5.0V		MIL		COM'L		
		Typ.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.	Typ.	Min. <sup>1</sup>	Max.	Min. <sup>1</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CPA, CPB to B <sub>n</sub> , A <sub>n</sub>	5.5 5.5	2.0 2.0	11.0 11.0	2.0 2.0	10.0 10.0	4.5 4.5	2.0 2.0	7.2 7.2	2.0 2.0	6.5 6.5	ns ns	1 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEA or OEB to A <sub>n</sub> or B <sub>n</sub>	5.5 5.5	1.5 1.5	13.0 13.0	1.5 1.5	10.5 10.5	4.5 4.5	1.5 1.5	7.5 7.5	1.5 1.5	6.5 6.5	ns ns	1,7 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Enable Time OEA or OEB to A <sub>n</sub> or B <sub>n</sub>	5.5 5.5	1.5 1.5	10.0 10.0	1.5 1.5	10.0 10.0	4.0 4.0	1.5 1.5	6.5 6.5	1.5 1.5	5.5 5.5	ns ns	1,7 8

Note: AC Characteristics guaranteed with C<sub>L</sub> = 50pF as shown in Figure 1.

1568 Tbl 10

AC OPERATING REQUIREMENTS

Sym	Parameter	P29PCT52A/53A					P29PCT52B/53B					Units	Fig. No.
		T <sub>A</sub> =+25°C V <sub>CC</sub> =+5.0V		MIL		COM'L	T <sub>A</sub> =+25°C V <sub>CC</sub> =+5.0V		MIL		COM'L		
		Typ.	Min.	Max.	Min.	Max.	Typ.	Min.	Max.	Min.	Max.		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW, A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	1.0 1.0	2.5 2.5		2.0 2.0		1.0 1.0	2.0 2.0		2.0 2.0		ns ns	4
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW, A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	0.5 0.5	2.0 2.0		2.0 2.0		0.5 0.5	1.5 1.5		1.5 1.5		ns ns	4
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set-up Time, HIGH or LOW, OEA, OEB to CPA, CPB	— —	2.0 2.0		2.0 2.0		— —	2.0 2.0		2.0 2.0		ns ns	4
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW, OEA, OEB to CPA, CPB	— —	2.0 2.0		2.0 2.0		— —	2.0 2.0		2.0 2.0		ns ns	4
t <sub>w</sub> (H) t <sub>w</sub> (L)	Pulse Width, HIGH or LOW, CPA or CPB	— —	3.0 3.0		3.0 3.0		— —	3.0 3.0		3.0 3.0		ns ns	5

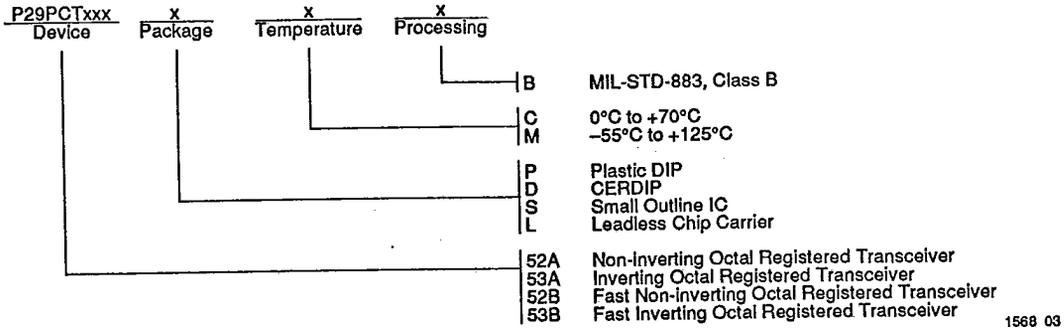
Note: Minimum limits are guaranteed but not tested on Propagation Delays.

1568 Tbl 11

4

T-52-31

ORDERING INFORMATION



TECHDOC 1568