

Electrical Specifications at 25°C

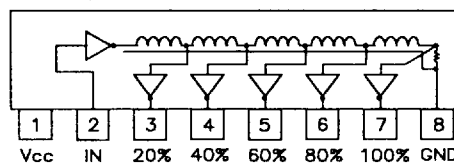
Delay Tolerances		TTL Buffered	FAST Buffered
Total (ns)	Tap-to-Tap (ns)	5 Tap SIP P/N	5 Tap SIP P/N
9 ± 1.00	** 1 ± 0.5	** SIDM-9	-----
13 ± 2.00	** 2 ± 1.0	** SIDM-13	-----
17 ± 2.00	** 3 ± 1.0	** SIDM-17	-----
25 ± 2.00	5 ± 2.0	SIDM-25	FSIDM-25
30 ± 2.00	6 ± 2.0	SIDM-30	FSIDM-30
35 ± 2.00	7 ± 2.0	SIDM-35	FSIDM-35
40 ± 2.00	8 ± 2.0	SIDM-40	FSIDM-40
45 ± 2.25	9 ± 2.0	SIDM-45	FSIDM-45
50 ± 2.50	10 ± 2.0	SIDM-50	FSIDM-50
60 ± 3.00	12 ± 2.0	SIDM-60	FSIDM-60
75 ± 3.75	15 ± 2.5	SIDM-75	FSIDM-75
80 ± 4.00	16 ± 2.5	SIDM-80	FSIDM-80
100 ± 5.00	20 ± 3.0	SIDM-100	FSIDM-100
125 ± 6.25	25 ± 3.0	SIDM-125	FSIDM-125
150 ± 7.50	30 ± 3.0	SIDM-150	FSIDM-150
200 ± 10.00	40 ± 4.0	SIDM-200	FSIDM-200
250 ± 12.50	50 ± 5.0	SIDM-250	FSIDM-250

** These part numbers do not have 5 equal taps. Specified Tap-to-Tap Delays are referenced to Tap 1: 5 ± 2 ns.

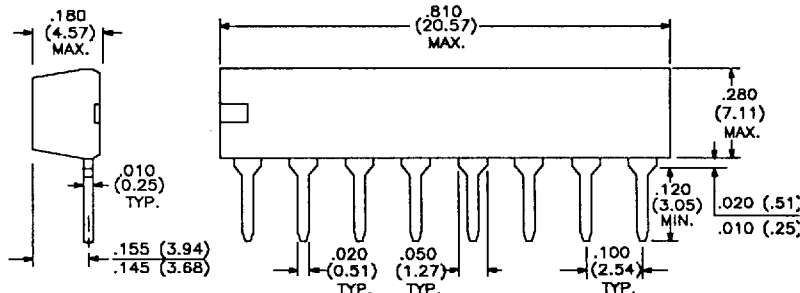
TTL Buffered 5-Tap SIP Delays

See "GENERAL" notes below.

5-Tap SIP Delay Schematic Diagram



PHYSICAL DIMENSIONS inches (mm)

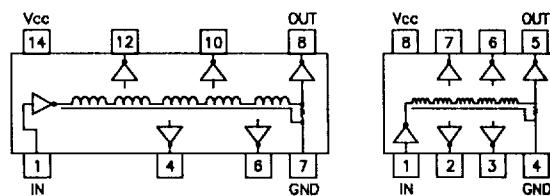


Single Output TTL / FAST / HC / ACT Buffered Delay Modules

Electrical Specifications at 25°C

Delay Tolerance (ns)	TTL Buffered Single		FAST	HC Buffered	ACT Buffered
	14 Pin Part Number	8 Pin Part Number	8 Pin Part Number	8 Pin Part Number	8 Pin Part Number
4 ± 1.00	-----	-----	FAMD-4	-----	-----
5 ± 1.00	AIDL-5	AMDL-5	FAMD-5	-----	-----
6 ± 1.00	AIDL-6	AMDL-6	FAMD-6	-----	-----
7 ± 1.00	AIDL-7	AMDL-7	FAMD-7	-----	-----
8 ± 1.00	AIDL-8	AMDL-8	FAMD-8	-----	ACMDL-8
9 ± 1.00	AIDL-9	AMDL-9	FAMD-9	-----	ACMDL-9
10 ± 1.50	AIDL-10	AMDL-10	FAMD-10	HCMDL-10	ACMDL-10
11 ± 1.50	AIDL-11	AMDL-11	FAMD-11	HCMDL-11	ACMDL-11
12 ± 1.50	AIDL-12	AMDL-12	FAMD-12	HCMDL-12	ACMDL-12
15 ± 1.50	AIDL-15	AMDL-15	FAMD-15	HCMDL-15	ACMDL-15
16 ± 1.50	AIDL-16	AMDL-16	FAMD-16	HCMDL-16	ACMDL-16
20 ± 2.00	AIDL-20	AMDL-20	FAMD-20	HCMDL-20	ACMDL-20
25 ± 2.00	AIDL-25	AMDL-25	FAMD-25	HCMDL-25	ACMDL-25
30 ± 2.00	AIDL-30	AMDL-30	FAMD-30	HCMDL-30	ACMDL-30
40 ± 2.00	AIDL-40	AMDL-40	FAMD-40	HCMDL-40	ACMDL-40
45 ± 2.25	AIDL-45	AMDL-45	FAMD-45	HCMDL-45	ACMDL-45
50 ± 2.50	AIDL-50	AMDL-50	FAMD-50	HCMDL-50	ACMDL-50
60 ± 3.00	AIDL-60	AMDL-60	FAMD-60	HCMDL-60	ACMDL-50
75 ± 3.75	AIDL-75	AMDL-75	FAMD-75	HCMDL-75	ACMDL-75
80 ± 4.00	AIDL-80	AMDL-80	FAMD-80	HCMDL-80	ACMDL-80
100 ± 5.00	AIDL-100	AMDL-100	FAMD-100	HCMDL-100	ACMDL-100
150 ± 7.50	AIDL-150	AMDL-150	FAMD-150	HCMDL-150	ACMDL-150
200 ± 10.00	AIDL-200	AMDL-200	FAMD-200	HCMDL-200	ACMDL-200
250 ± 12.50	AIDL-250	AMDL-250	FAMD-250	-----	-----
500 ± 25.00	AIDL-500	AMDL-500	FAMD-500	-----	-----

Single Delay Schematic Diagrams



GENERAL: For Operating Specifications and Test Conditions, see Tables I, II, III, VII & IX on page 7 of this catalog, as applicable. Delays Specified for the Leading Edge.

Tap Delays referenced to Input ± 5% or ± 2 ns
 Minimum Input Pulse Width 40% of total delay
 Temperature Coefficient 500ppm/°C typical
 Supply Current, I_{cc} :
 AIDL, AMDL, SIDM 39 mA typ., 65 mA max.
 FAMD, FSIDM 25 mA typ., 48 mA max.
 HCMDL 10 mA typ., 15 mA max.
 ACMDL 22 mA typ., 44 mA max.

PHYSICAL DIMENSIONS:

8 Pin & 14 Pin DIP & SMD G or J See Page 16
 AIDL will have unused pins removed as per schematic diagram.

SMD PART NUMBERS: Part numbers from Table are for DIP style. For SMD styles, the appropriate Suffix (G or J) is amended to base part number from table. Example:
 DIP AMDL-25
 SMD G AMDL-25G
 SMD J AMDL-25J

VARIATIONS AVAILABLE. FOR INTERMEDIATE VALUES AND/OR CUSTOM DESIGNS PLEASE CONSULT THE FACTORY.

Specifications subject to change without notice.

AIDL-6/93

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