REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Editorial changes throughout. Convert to military drawing format. Added vendor CAGE numbers 27014 and 18324. Table I, propagation delay changes.	88-05-03	Michael A. Frye
D	Changes in accordance with NOR 5962-R080-92. Changes to Table I and Figure 4.	92-07-06	Monica L. Poelking
E	Changes in accordance with NOR 5962-R136-96. Changes to Device Type 02 adding suffix "A" and Table 1. -les	96-06-05	Michael A. Frye
F	Editorial changes throughout. Table 1, propagation delay changes. -les	97-10-28	Raymond Monnin

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	F																			
SHEET	15																			

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
David H. Johnson

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
84-03- 07

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, ADVANCED LOW POWER SCHOTTKY TTL, FLIP-FLOPS,MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**83020**

SHEET 1 OF 15

DSSC FORM 2233
APR 97

5962-E030-98

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part number. The complete part number shall be as shown in the following example:

83020	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS373	Octal, D-type, flip-flop with transparent latch and 3-state outputs
02	54ALS374A	Octal, D-type, edge-triggered, flip-flop with 3-state outputs

1.2.2 Case outlines. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or GDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or GDFP3-F20	20	Flat
2	CQCC1-N20	20	Square chip carrier

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range(V_{CC})	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range(V_I)	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 4/:	
Device type 01	148.5 mW
Device type 02	170.5 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C. Unused inputs must be held high or low.
4/ Maximum power dissipation is defined as V_{CC} x I_{CC} and must withstand the added P_D due to short-circuit test, e.g., I_O.

1.4 Recommended operating conditions - continued.

Maximum low level input voltage (V_{IL}):	
T_C = +125°C	0.7 V dc
T_C = -55°C	0.8 V dc
T_C = +25°C	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Normalized fanout (each output):	
At low logic level	10 maximum
At high logic level	20 maximum
Minimum width of clock pulse (t_p(clk)):	
Device type 02	
at +25°C	14 ns
at -55°C and +125°C	16.5 ns
Minimum width of Enable pulse (t_p(Enable)):	
Device type 01	12 ns
Minimum setup time before clock (^{t}setup):	
Device type 02	10 ns
Minimum hold time after clock (^{t}hold):	
Device type 02	4 ns
Minimum setup time before Enable (^{t}setup):	
Device type 01	10 ns
Minimum hold time after Enable (^{t}hold):	
Device type 01	7 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. Tthe following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connection(s). The terminal connection(s) shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.5 Switching waveform(s) and test circuit. The switching waveform(s) and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	Data input = 2.0 V OC input ≤ 0.7 V V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} at: 2/ +125°C = 0.7 V dc -55°C = 0.8 V dc +25°C = 0.8 V dc I_{OH} = -0.4 mA I_{OH} = -1.0 mA	All	1,2,3	2.5 2.4		V
Low level output voltage	V_{OL}	V_{IL} at: Data input = 0.7 V +125°C = 0.7 V 2/ -55°C = 0.8 V OC input ≤ 0.7 V +25°C = 0.8 V V_{CC} = 4.5 V I_{OL} = 12 mA V_{IH} = 2.0 V	All	1,2,3		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA	All	1,2,3		-1.5	V
Low level input current	I_{IL}	V_{IN} = 0.4 V V_{CC} = 5.5 V All other inputs = 4.5 V	01 02	1,2,3		-100 -200	µA
High level input current	I_{IH1}	V_{CC} = 5.5 V; V_{IN} = 2.7 V All other inputs = 0.0 V	All	1,2,3		20	µA
	I_{IH2}	V_{CC} = 5.5 V; V_{IN} = 7.0 V All other inputs = 0.0 V				0.1	mA
Output current	I_O	V_{CC} = 5.5 V V_{OUT} = 2.25 V 3/	All	1,2,3	-20	-112	mA
Off-state output current	I_{OZH}	V_{CC} = 5.5 V V_{OUT} = 2.7 V	All	1,2,3		20	µA
	I_{OZL}	V_{CC} = 5.5 V V_{OUT} = 0.4 V	All	1,2,3		-20	µA
Supply current, outputs high	I_{CCH}	$V_{IN} \ge 4.5$ V V_{CC} = 5.5 V	01 02	1,2,3		16 21	mA mA
Supply current, outputs low	I_{CCL}	$V_{IN} \le 0.4$ V V_{CC} = 5.5 V	01 02	1,2,3		25 28	mA mA
Supply current, outputs disabled	I_{CCZ}	V_{CC} = 5.5 V	01 02	1,2,3		27 31	mA mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Functional tests		See 4.3.1c 4/	All	7,8			
Maximum clock frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF ±10% R_1 = 500Ω ±5% 5/ R_2 = 500Ω ±5% See figure 4	All	9,10,11	30		MHz
Propagation delay time, CLK to Q	t_{PLH1}		02	9,10,11	3	14	ns
	t_{PHL1}		02	9,10,11	5	17	ns
Propagation delay time, D to Q	t_{PLH2}		01	9,10,11	2	14	ns
	t_{PHL2}		01	9,10,11	1	17	ns
Propagation delay time, G to Q	t_{PLH3}		01	9,10,11	6	26	ns
	t_{PHL3}		01	9,10,11	1	23	ns
Enable time, from OC to Q	t_{PZH}		01	9,10,11	3	18.5	ns
			02		3	18	ns
	t_{PZL}		01	9,10,11	3	20.5	ns
			02		5	21	ns
Disable time, from OC to Q	t_{PHZ}		01	9,10,11	2	13.5	ns
			02		1	11	ns
	t_{PLZ}		01	9,10,11	2	20	ns
			02		2	19	ns

1/ Unused inputs that do not directly control the pin under test must be put ≥ 2.5 V or ≤ 0.4 V, and shall not exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or V_{IH} minimum input.

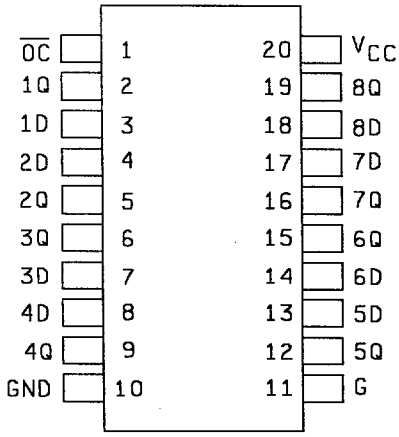
3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. Not more than one output will be tested at a time and the duration of the test condition shall not exceed one second.

4/ Functional tests shall be conducted at input test conditions of $0.0 V \le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

5/ The propagation delay limits are based on single output switching. Unused inputs = 3.5 V or 0.3 V.

Device type 01

CASE R AND S



CASE 2

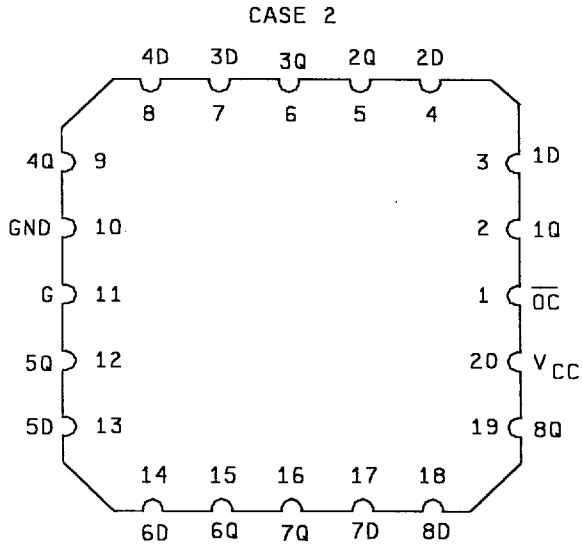
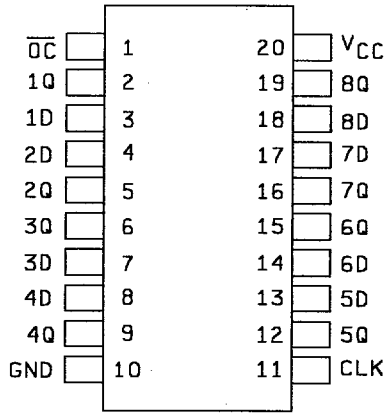


FIGURE 1. Terminal connections (top views).

STANDARDIZED MILITARY DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE A		83020
		REVISION LEVEL F	SHEET 7

Device type 02

CASE R AND S



CASE 2

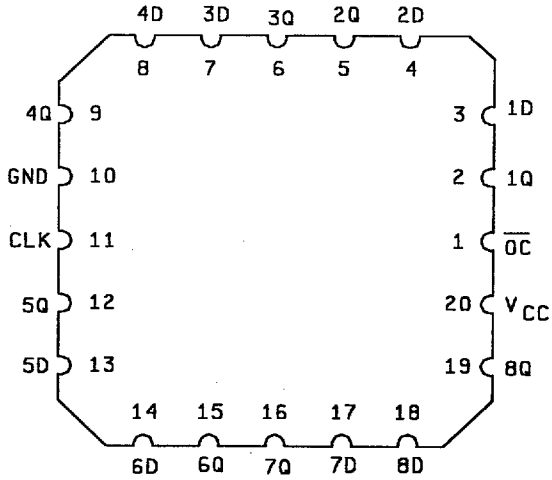


FIGURE 1. Terminal connections (top views) - Continued.

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Device type 01

Input			Output
$\overline{OC}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Device type 02

Input			Output
$\overline{OC}$	G	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low level
H = High level
X = Irrelevant
↑ = Transition from low to high level
Z = Off state of three-state output
Q_0 = Level of Q before the steady-state input conditions were established

FIGURE 2. Truth tables.

Device type 01

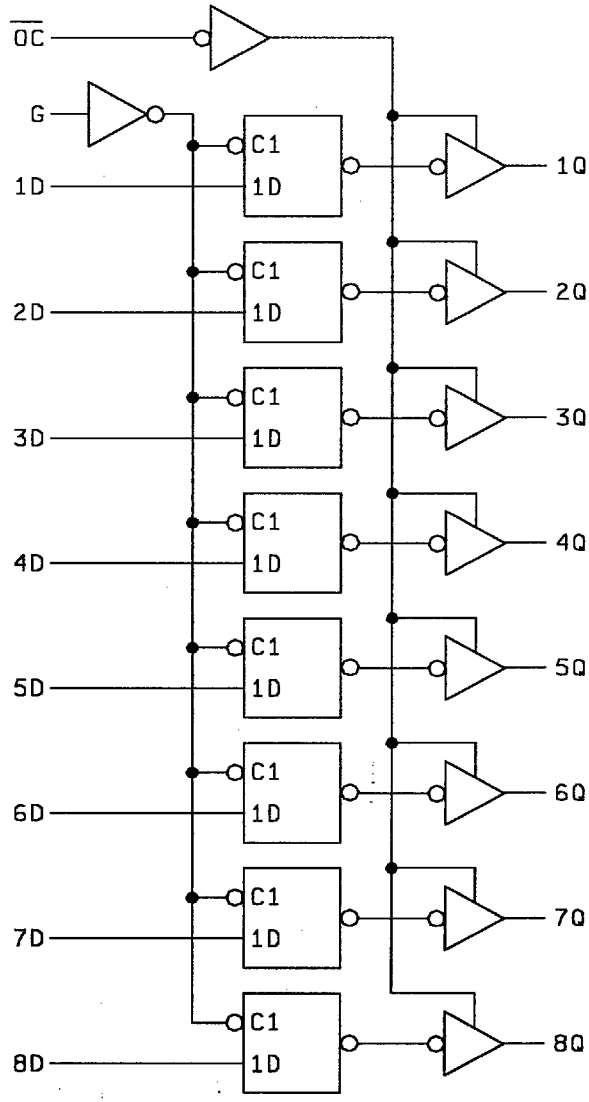

FIGURE 3. Logic dagrams

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Device type 02

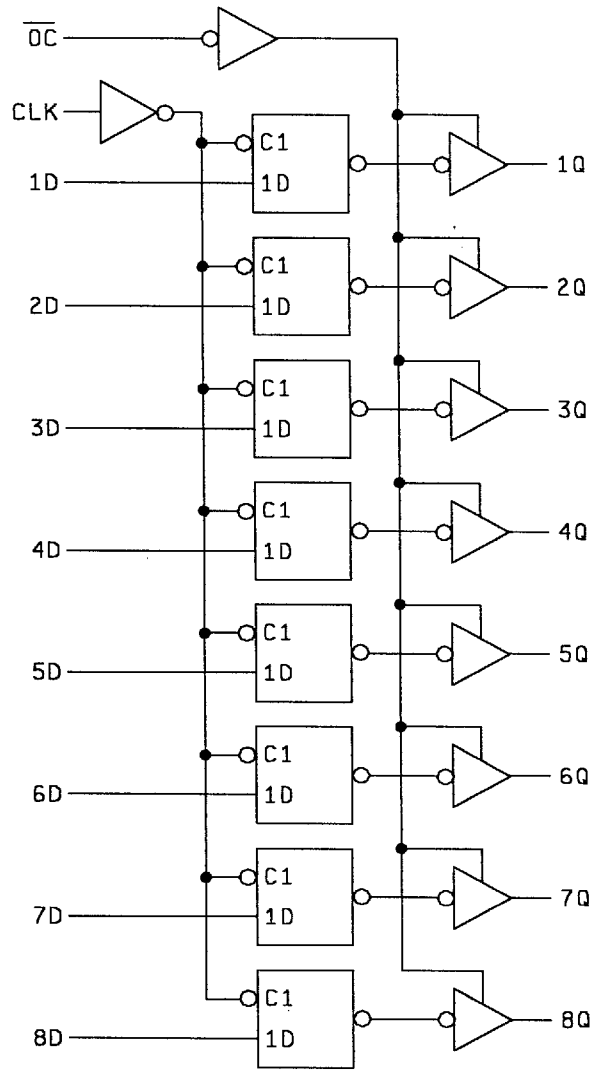
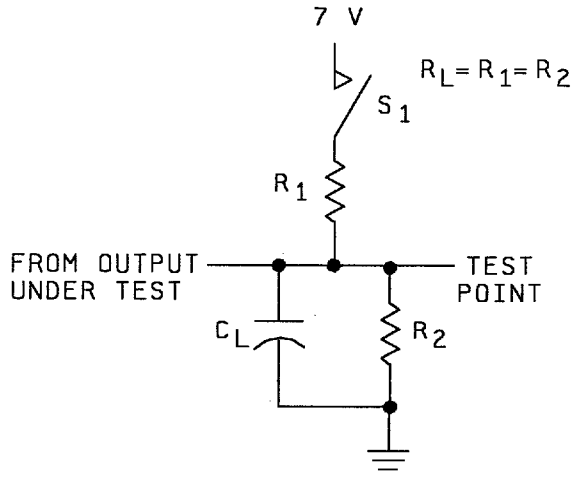
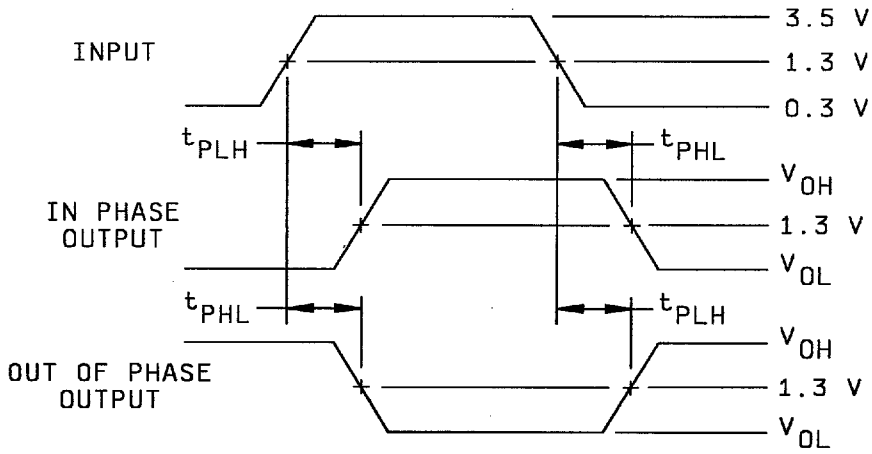


FIGURE 3. Logic diagrams - Continued.

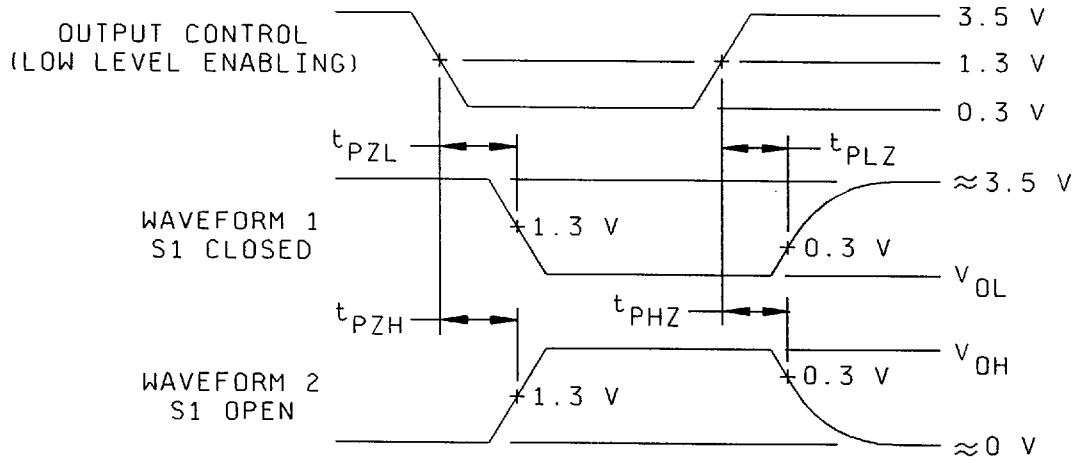


LOAD CIRCUIT
FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 4. Switching waveforms and test circuit.



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUT

NOTES:
1. C_L includes probe and jig capacitiance.
2. When measuring propagation delay times of three-state outputs, switch S1 is open.
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input pulses have the following characteristics: PRR ≤10 Mhz, duty cycle = 50%, $t_r = t_f = 3$ ns ±1 ns.
5. The outputs are measured one at a time with one input transistion per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or . The test circuit shall be maintained by the manufacturer under the document revision level control and shall be made available to the preparing or acquiring activity upon request. The testcircuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883,method 5005, table 1)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9,10,11
Group A test requirements (method 5005)	1,2,3,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A or D. The test circuit shall be maintained by themanufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificateof compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN
DATE: 97-10-28

Approved sources of supply for SMD 83020 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Military specification part number
8302001RA	01295	SNJ54ALS373J	M38510/37203BRA
8301001SA	01295	SNJ54ALS373W	M38510/37203BSA
83020012A	01295	SNJ54ALS373FK	M38510/37203B2A
8302002RA	01295	SNJ54ALS374AJ	M38510/37204BRA
8302002SA	01295	SNJ54ALS374AW	M38510/37204BSA
83020022A	01295	SNJ54ALS374AFK	M38510/37204B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.