PowerPC®

IBM

PowerPC 405x3 Embedded Cores

Low-cost, reusable, 200+ MHz cores for system on a chip applications

Highlights

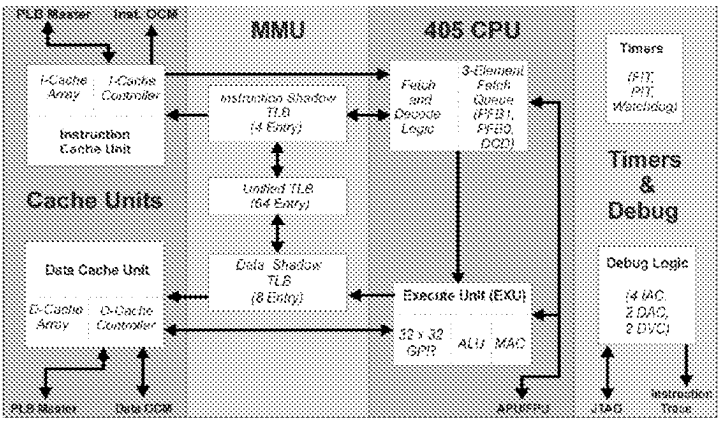
PowerPC® 405x3 embedded cores are 32-bit RISC cores for use in custom logic applications, as well as standard products from IBM®. These embedded cores integrate a PowerPC 405™ CPU, separate instruction and data caches, a JTAG port, trace FIFO, multiple timers and a memory management unit (MMU). These cores are available as hard macros in the IBM Blue Logic™ core library and can be integrated with peripheral and application-specific macro cores to develop system-on-a-chip solutions. PowerPC 405x3 cores are optimized for low-cost, low-power consumer electronics, communications, and pervasive computing applications.

The PowerPC 405 CPU is compatible with the scalable and flexible PowerPC instruction set architecture, so code written for a PowerPC 405x3 is compatible with 4xx, 6xx and 7xx PowerPC embedded processors. The PowerPC 405 CPU implements a simple 5-stage pipeline in order to minimize silicon area, thus optimizing system-on-a-chip designs for low cost.

For optimal performance and cost-control, the PowerPC 405x3 cores include tightly coupled features in addition to the 405 CPU. The cache controllers use sophisticated design techniques typically found in higher-performance devices. The MMU was designed for low-cost embedded applications due to its small size and flexibility. JTAG and Trace FIFO ports enable robust debug capabilities, even in complex system-on-a-chip designs.

PowerPC 405x3 embedded cores are supported by the PowerPC Embedded Tools Program. In this program, IBM and over 75 select third-party vendors offer a full range of embedded system development tools. Available tools include compilers, debuggers, real-time operating systems, hardware/software co-simulation environments, and logic analyzers.

Full-function simulation models are available to support all SWIFT compliant VHDL and Verilog simulation environments.



PowerPC 405 Core Block Diagram

405 CPU

- Compatible with PowerPC User Instruction Set Architecture
- Five-stage pipeline
- 32-bit x 32 general purpose registers
- Hardware multiply and divide
- Branch prediction

Cache Controllers

- Separate I- and D- cache units
- Fill-first, data forwarding
- Non-blocking flush operations
- Programmable loads and store

Virtual Mode MMU

- Variable page sizes (1 KB-16 MB)
- 64-entry fully-associative TLB

I/O Interfaces

- Processor Local Bus (PLB)
- Auxiliary Processing Unit (APU)
- On-Chip Memory (OCM)
- JTAG

Timers

- 64-bit time-base
- Programmable interval timer
- Fixed interval timer
- Watchdog timer

Debug Support

- 4 Instruction Address, 2 Data Address, and 2 Data Value breakpoints
- Real-time non-invasive trace
- Exclusive traceback capability

Specifications	405A3	405B3
Technology	.25µ CMOS (.18µ L_{eff})	.25µ CMOS (.18µ L_{eff})
Frequency (MHz)	0 to 210[WC] 0 to 300[TC]	0 to 210[WC] 0 to 300[TC]
Performance (Dhrystone 2.1 MIPS)	296@210MHz[WC] 423@300MHz[TC]	296@200MHz[WC] 423@300MHz[TC]
Power Dissipation (estimated, typical)	1W[TC]	650mW[TC]
Voltage	2.5V	2.5V
I-Cache	32K	16K
D-Cache	32K	8K
MMU	Y	Y
Timers	Y	Y
JTAG	Y	Y
Trace FIFO	Y	Y

[WC] Worst case conditions (2.3V, 85° C, slow silicon)

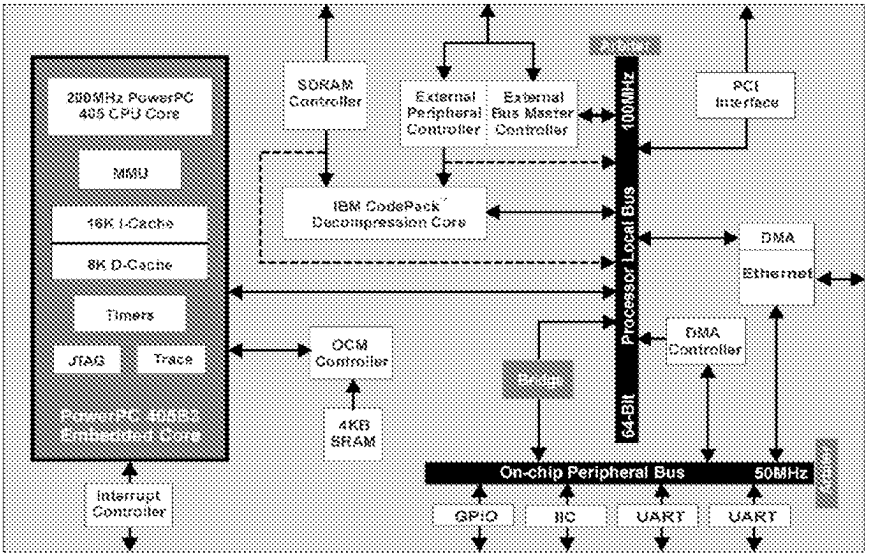
[TC] Typical conditions (2.5V, 55° C, nominal silicon)

405x3 Core Integration

Through the IBM CoreConnect™ bus architecture, PowerPC 405x3 CPU cores integrate on-chip with other reusable peripheral and application-specific cores. High speed, high bandwidth peripherals, such as the embedded controller core, directly attach to the processor local bus (PLB). Less performance-critical cores attach to the on-chip peripheral bus (OPB).

The PowerPC 405x3 cores and CoreConnect are part of Blue Logic superstructures, which help reduce time to market of SOC designs.

For more information on IBM Microelectronics core offerings, view the ever expanding core library at http://www.chips.ibm.com/products/asics/ or contact your local IBM Microelectronics sales office.



Example 405 Core Application

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