

## ★ FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 15/17/20/25/30/35 ns (Commercial)
  - 20/25/30/35/45 ns (Military)
- Low Power Operation (Commercial/Military)
  - 690 mW Active – 15,17
  - 605/715 mW Active – 20
  - 495/575 mW Active – 25, 30, 35, 45
  - 116/127 mW Standby (TTL Input)
  - 1.1 mW Standby (CMOS Input) P4C164L
- Output Enable and Dual Chlp Enable Control Functions
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply, 10 µA Typical Current
- Common Data I/O
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE II Technology™
- Standard Pinout (JEDEC Approved)
  - 28-Pin 300 mil DIP, SOJ
  - 28-Pin 600 mil ceramic DIP
  - 28-Pin 350 x 550 mil LCC

The P4C164 and P4C164L are available in 28-pin 300 mil DIP and SOJ, 28-pin 600 mil ceramic DIP, and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

The image shows two pin diagrams for the 28-pin 74VHC00. The left diagram is for DIP (P5, C5, D5-1) and SOJ (J5) packages, showing a notch at pin 1. The right diagram is for the LCC (L5) package, showing a square package with pins on all four sides. Pin numbers 1 through 28 are indicated for both diagrams.

**DIP (P5, C5, D5-1), SOJ (J5) TOP VIEW**

| Pin | Signal           | Pin | Signal           |
|-----|------------------|-----|------------------|
| 1   | NC               | 28  | V <sub>CC</sub>  |
| 2   | A <sub>0</sub>   | 27  | WE               |
| 3   | A <sub>1</sub>   | 26  | CE <sub>2</sub>  |
| 4   | A <sub>2</sub>   | 25  | A <sub>12</sub>  |
| 5   | A <sub>3</sub>   | 24  | A <sub>11</sub>  |
| 6   | A <sub>4</sub>   | 23  | A <sub>10</sub>  |
| 7   | A <sub>5</sub>   | 22  | OE               |
| 8   | A <sub>6</sub>   | 21  | A <sub>2</sub>   |
| 9   | A <sub>7</sub>   | 20  | CE <sub>1</sub>  |
| 10  | A <sub>8</sub>   | 19  | I/O <sub>8</sub> |
| 11  | I/O <sub>1</sub> | 18  | I/O <sub>7</sub> |
| 12  | I/O <sub>2</sub> | 17  | I/O <sub>6</sub> |
| 13  | I/O <sub>3</sub> | 16  | I/O <sub>5</sub> |
| 14  | GND              | 15  | I/O <sub>4</sub> |

**LCC (L5) TOP VIEW**

| Pin | Signal            | Pin | Signal            |
|-----|-------------------|-----|-------------------|
| 31  | A <sub>2</sub>    | 27  | WE                |
| 30  | A <sub>1</sub>    | 26  | CE <sub>2</sub>   |
| 29  | A <sub>0</sub>    | 25  | A <sub>12</sub>   |
| 28  | V <sub>CC</sub>   | 24  | A <sub>11</sub>   |
| 27  | NC                | 23  | A <sub>10</sub>   |
| 26  | A <sub>3</sub>    | 22  | OE                |
| 25  | A <sub>4</sub>    | 21  | A <sub>2</sub>    |
| 24  | A <sub>5</sub>    | 20  | CE <sub>1</sub>   |
| 23  | A <sub>6</sub>    | 19  | A <sub>9</sub>    |
| 22  | A <sub>7</sub>    | 18  | I/O <sub>8</sub>  |
| 21  | A <sub>8</sub>    | 17  | I/O <sub>7</sub>  |
| 20  | A <sub>9</sub>    | 16  | I/O <sub>6</sub>  |
| 19  | I/O <sub>1</sub>  | 15  | I/O <sub>5</sub>  |
| 18  | I/O <sub>2</sub>  | 14  | I/O <sub>4</sub>  |
| 17  | I/O <sub>3</sub>  | 13  | I/O <sub>3</sub>  |
| 16  | GND               | 12  | GND               |
| 15  | I/O <sub>4</sub>  | 11  | I/O <sub>4</sub>  |
| 14  | I/O <sub>5</sub>  | 10  | I/O <sub>5</sub>  |
| 13  | I/O <sub>6</sub>  | 9   | I/O <sub>6</sub>  |
| 12  | I/O <sub>7</sub>  | 8   | I/O <sub>7</sub>  |
| 11  | I/O <sub>8</sub>  | 7   | I/O <sub>8</sub>  |
| 10  | I/O <sub>9</sub>  | 6   | I/O <sub>9</sub>  |
| 9   | I/O <sub>10</sub> | 5   | I/O <sub>10</sub> |
| 8   | I/O <sub>11</sub> | 4   | I/O <sub>11</sub> |
| 7   | I/O <sub>12</sub> | 3   | I/O <sub>12</sub> |
| 6   | I/O <sub>13</sub> | 2   | I/O <sub>13</sub> |
| 5   | I/O <sub>14</sub> | 1   | I/O <sub>14</sub> |
| 4   | I/O <sub>15</sub> | 0   | I/O <sub>15</sub> |
| 3   | I/O <sub>16</sub> | -1  | I/O <sub>16</sub> |
| 2   | I/O <sub>17</sub> | -2  | I/O <sub>17</sub> |
| 1   | I/O <sub>18</sub> | -3  | I/O <sub>18</sub> |
| 0   | I/O <sub>19</sub> | -4  | I/O <sub>19</sub> |
| -1  | I/O <sub>20</sub> | -5  | I/O <sub>20</sub> |
| -2  | I/O <sub>21</sub> | -6  | I/O <sub>21</sub> |
| -3  | I/O <sub>22</sub> | -7  | I/O <sub>22</sub> |
| -4  | I/O <sub>23</sub> | -8  | I/O <sub>23</sub> |
| -5  | I/O <sub>24</sub> | -9  | I/O <sub>24</sub> |
| -6  | I/O <sub>25</sub> | -10 | I/O <sub>25</sub> |
| -7  | I/O <sub>26</sub> | -11 | I/O <sub>26</sub> |
| -8  | I/O <sub>27</sub> | -12 | I/O <sub>27</sub> |
| -9  | I/O <sub>28</sub> | -13 | I/O <sub>28</sub> |
| -10 | I/O <sub>29</sub> | -14 | I/O <sub>29</sub> |
| -11 | I/O <sub>30</sub> | -15 | I/O <sub>30</sub> |
| -12 | I/O <sub>31</sub> | -16 | I/O <sub>31</sub> |
| -13 | I/O <sub>32</sub> | -17 | I/O <sub>32</sub> |
| -14 | I/O <sub>33</sub> | -18 | I/O <sub>33</sub> |
| -15 | I/O <sub>34</sub> | -19 | I/O <sub>34</sub> |
| -16 | I/O <sub>35</sub> | -20 | I/O <sub>35</sub> |
| -17 | I/O <sub>36</sub> | -21 | I/O <sub>36</sub> |
| -18 | I/O <sub>37</sub> | -22 | I/O <sub>37</sub> |
| -19 | I/O <sub>38</sub> | -23 | I/O <sub>38</sub> |
| -20 | I/O <sub>39</sub> | -24 | I/O <sub>39</sub> |
| -21 | I/O <sub>40</sub> | -25 | I/O <sub>40</sub> |
| -22 | I/O <sub>41</sub> | -26 | I/O <sub>41</sub> |
| -23 | I/O <sub>42</sub> | -27 | I/O <sub>42</sub> |
| -24 | I/O <sub>43</sub> | -28 | I/O <sub>43</sub> |
| -25 | I/O <sub>44</sub> | -29 | I/O <sub>44</sub> |
| -26 | I/O <sub>45</sub> | -30 | I/O <sub>45</sub> |
| -27 | I/O <sub>46</sub> | -31 | I/O <sub>46</sub> |
| -28 | I/O <sub>47</sub> | -32 | I/O <sub>47</sub> |
| -29 | I/O <sub>48</sub> | -33 | I/O <sub>48</sub> |
| -30 | I/O <sub>49</sub> | -34 | I/O <sub>49</sub> |
| -31 | I/O <sub>50</sub> | -35 | I/O <sub>50</sub> |
| -32 | I/O <sub>51</sub> | -36 | I/O <sub>51</sub> |
| -33 | I/O <sub>52</sub> |     |                   |

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MAXIMUM RATINGS<sup>(1)</sup>

| Symbol     | Parameter                                         | Value                  | Unit |
|------------|---------------------------------------------------|------------------------|------|
| $V_{CC}$   | Power Supply Pin with Respect to GND              | -0.5 to +7             | V    |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to $V_{CC} + 0.5$ | V    |
| $T_A$      | Operating Temperature                             | -55 to +125            | °C   |

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| Symbol     | Parameter              | Value       | Unit |
|------------|------------------------|-------------|------|
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C   |
| $T_{STG}$  | Storage Temperature    | -65 to +150 | °C   |
| $P_T$      | Power Dissipation      | 1.0         | W    |
| $I_{OUT}$  | DC Output Current      | 50          | mA   |

1519 Tbl 02

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Military             | -55 to +125°C       | 0V  | 5.0V ± 10% |

1519 Tbl 03

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Commercial           | 0°C to +70°C        | 0V  | 5.0V ± 10% |

1519 Tbl 04

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol           | Parameter                          | Test Conditions                                                                                                      | P4C164               |                      | P4C164L              |                      | Unit |
|------------------|------------------------------------|----------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------|----------------------|------|
|                  |                                    |                                                                                                                      | Min                  | Max                  | Min                  | Max                  |      |
| V <sub>IH</sub>  | Input High Voltage                 |                                                                                                                      | 2.2                  | V <sub>CC</sub> +0.5 | 2.2                  | V <sub>CC</sub> +0.5 | V    |
| V <sub>IL</sub>  | Input Low Voltage                  |                                                                                                                      | -0.5 <sup>(3)</sup>  | 0.8                  | -0.5 <sup>(3)</sup>  | 0.8                  | V    |
| V <sub>HG</sub>  | CMOS Input High Voltage            |                                                                                                                      | V <sub>CC</sub> -0.2 | V <sub>CC</sub> +0.5 | V <sub>CC</sub> -0.2 | V <sub>CC</sub> +0.5 | V    |
| V <sub>LG</sub>  | CMOS Input Low Voltage             |                                                                                                                      | -0.5 <sup>(3)</sup>  | 0.2                  | -0.5 <sup>(3)</sup>  | 0.2                  | V    |
| V <sub>CD</sub>  | Input Clamp Diode Voltage          | V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA                                                                     |                      | -1.2                 |                      | -1.2                 | V    |
| V <sub>OL</sub>  | Output Low Voltage<br>(TTL Load)   | I <sub>OL</sub> = +10 mA, V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = +8 mA, V <sub>CC</sub> = Min.                  |                      | 0.5<br>0.4           |                      | 0.5<br>0.4           | V    |
| V <sub>OLC</sub> | Output Low Voltage<br>(CMOS Load)  | I <sub>OLC</sub> = +100 μA, V <sub>CC</sub> = Min.                                                                   |                      | 0.2                  |                      | 0.2                  | V    |
| V <sub>OH</sub>  | Output High Voltage<br>(TTL Load)  | I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.                                                                      | 2.4                  |                      | 2.4                  |                      | V    |
| V <sub>OHC</sub> | Output High Voltage<br>(CMOS Load) | I <sub>OHC</sub> = -100 μA, V <sub>CC</sub> = Min.                                                                   | V <sub>CC</sub> -0.2 |                      | V <sub>CC</sub> -0.2 |                      | V    |
| I <sub>LI</sub>  | Input Leakage Current              | V <sub>CC</sub> = Max. Mil.<br>V <sub>IN</sub> = GND to V <sub>CC</sub> Com'l.                                       | -10<br>-5            | +10<br>+5            | -5<br>-2             | +5<br>+2             | μA   |
| I <sub>LO</sub>  | Output Leakage Current             | V <sub>CC</sub> = Max., $\overline{CE}$ = V <sub>IH</sub> , Mil.<br>V <sub>OUT</sub> = GND to V <sub>CC</sub> Com'l. | -10<br>-5            | +10<br>+5            | -5<br>-2             | +5<br>+2             | μA   |

1519 Tbl 05

CAPACITANCES<sup>(4)</sup> $(V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}, f = 1.0\text{MHz})$ 

| Symbol   | Parameter         | Conditions           | Typ. | Unit |
|----------|-------------------|----------------------|------|------|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0\text{V}$ | 5    | pF   |

1519 Tbl 06

| Symbol    | Parameter          | Conditions            | Typ. | Unit |
|-----------|--------------------|-----------------------|------|------|
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0\text{V}$ | 7    | pF   |

1519 Tbl 07

## Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with  $V_{IH}$  and  $I_{IL}$  not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

## POWER DISSIPATION CHARACTERISTICS

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Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol    | Parameter                                        | Test Conditions                                                                                                                                                     | P4C164 |            | P4C164L |            | Unit |
|-----------|--------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------|---------|------------|------|
|           |                                                  |                                                                                                                                                                     | Min    | Max        | Min     | Max        |      |
| $I_{CC}$  | Dynamic Operating Current – 15, 17               | $V_{CC} = \text{Max.}, f = \text{Max.},$ Mil.<br>Outputs Open Com'l.                                                                                                | —      | n/a<br>125 | —       | n/a<br>n/a | mA   |
| $I_{CC}$  | Dynamic Operating Current – 20                   | $V_{CC} = \text{Max.}, f = \text{Max.},$ Mil.<br>Outputs Open Com'l.                                                                                                | —      | 130<br>110 | —       | 130<br>110 | mA   |
| $I_{CC}$  | Dynamic Operating Current – 25, 30, 35, 45       | $V_{CC} = \text{Max.}, f = \text{Max.},$ Mil.<br>Outputs Open Com'l.                                                                                                | —      | 105<br>90  | —       | 105<br>90  | mA   |
| $I_{SB}$  | Standby Power Supply Current (TTL Input Levels)  | $\overline{CE}_1 \geq V_{IH}$ or<br>$CE_2 \leq V_{IL}, V_{CC} = \text{Max.},$ Mil.<br>$f = \text{Max.},$ Outputs Open Com'l.                                        | —      | 23<br>21   | —       | 23<br>21   | mA   |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}_1 \geq V_{HC}$ or<br>$CE_2 \leq V_{LC}, V_{CC} = \text{Max.},$ Mil.<br>$f = 0,$ Outputs Open, Com'l.<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | —      | 18<br>17   | —       | 1<br>0.2   | mA   |

n/a = Not Applicable

1519 Tbl 08

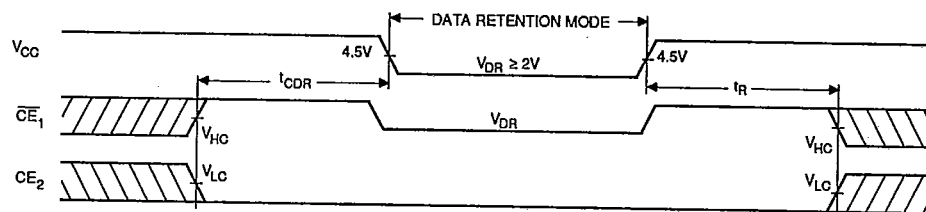
## DATA RETENTION CHARACTERISTICS (P4C164L Only)

| Symbol        | Parameter                            | Test Condition                                                                         | Min               | Typ.*<br>$V_{CC} =$ |          | Max<br>$V_{CC} =$ |           | Unit               |
|---------------|--------------------------------------|----------------------------------------------------------------------------------------|-------------------|---------------------|----------|-------------------|-----------|--------------------|
|               |                                      |                                                                                        |                   | 2.0V                | 3.0V     | 2.0V              | 3.0V      |                    |
| $V_{DR}$      | $V_{CC}$ for Data Retention          |                                                                                        | 2.0               |                     |          |                   |           | V                  |
| $I_{CCDR}$    | Data Retention Current               | Mil.<br>Com'l.                                                                         |                   | 10<br>10            | 15<br>15 | 200<br>60         | 300<br>90 | $\mu A$<br>$\mu A$ |
| $t_{CDR}$     | Chip Deselect to Data Retention Time | $\overline{CE}_1 \geq V_{CC} - 0.2V$ or<br>$CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ | 0                 |                     |          |                   |           | ns                 |
| $t_R^\dagger$ | Operation Recovery Time              | or $V_{IN} \leq 0.2V$                                                                  | $t_{RC}^\ddagger$ |                     |          |                   |           | ns                 |

\* $T_A = +25^\circ C$  $t_{RC}^\ddagger$  = Read Cycle Time $^\dagger$  This parameter is guaranteed but not tested.

1519 Tbl 09

## DATA RETENTION WAVEFORM



1519 01



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# AC ELECTRICAL CHARACTERISTICS—READ CYCLE

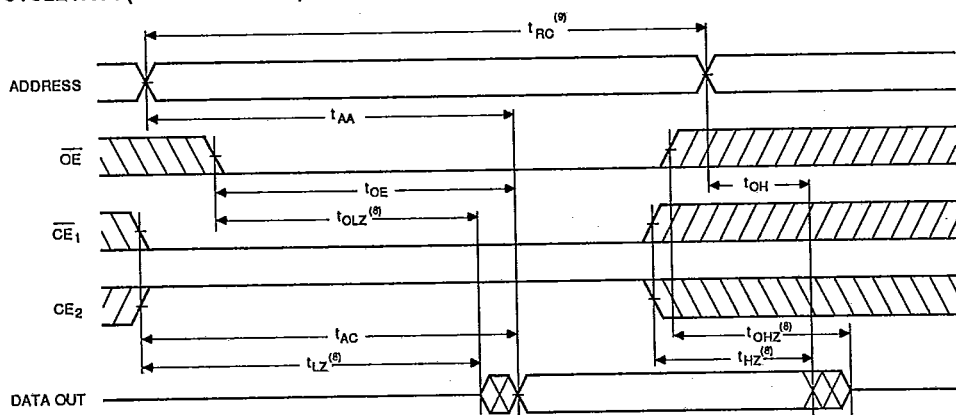
(V<sub>CC</sub> = 5V ± 10%, All Temperature Ranges)<sup>(2)</sup>

| Sym.             | Parameter                        | -15* |     | -17 |     | -20 |     | -25 |     | -30 |     | -35 |     | -45 |     | Unit |
|------------------|----------------------------------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|                  |                                  | Min  | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| t <sub>RC</sub>  | Read Cycle Time                  | 15   |     | 17  |     | 20  |     | 25  |     | 30  |     | 35  |     | 45  |     | ns   |
| t <sub>AA</sub>  | Address Access Time              |      | 15  |     | 17  |     | 20  |     | 25  |     | 30  |     | 35  |     | 45  | ns   |
| t <sub>AC</sub>  | Chip Enable Access Time          |      | 15  |     | 17  |     | 20  |     | 25  |     | 30  |     | 35  |     | 45  | ns   |
| t <sub>OH</sub>  | Output Hold from Address Change  | 2    |     | 2   |     | 2   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| t <sub>LZ</sub>  | Chip Enable to Output in Low Z   | 2    |     | 2   |     | 2   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| t <sub>HZ</sub>  | Chip Disable to Output in High Z |      | 8   |     | 8   |     | 8   |     | 10  |     | 13  |     | 15  |     | 20  | ns   |
| t <sub>OE</sub>  | Output Enable Low to Data Valid  |      | 9   |     | 10  |     | 10  |     | 13  |     | 15  |     | 18  |     | 20  | ns   |
| t <sub>OLZ</sub> | Output Enable Low to Low Z       | 2    |     | 2   |     | 2   |     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| t <sub>OHZ</sub> | Output Enable High to High Z     |      | 9   |     | 9   |     | 9   |     | 12  |     | 14  |     | 15  |     | 20  | ns   |
| t <sub>PU</sub>  | Chip Enable to Power Up Time     | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| t <sub>PD</sub>  | Chip Disable to Power Down Time  |      | 15  |     | 17  |     | 20  |     | 20  |     | 20  |     | 20  |     | 25  | ns   |

\*V<sub>CC</sub> = 5V ± 5% for -15

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## READ CYCLE NO. 1 (OE CONTROLLED)<sup>(5)</sup>



1519 02

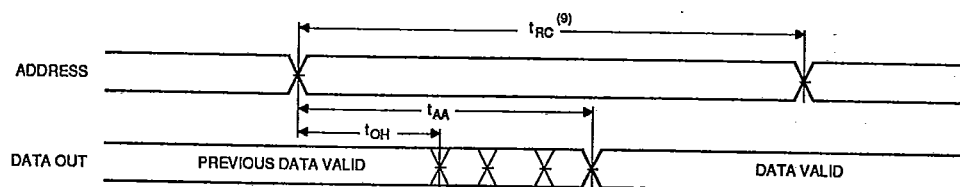
### Notes:

- WE is high for READ cycle.
- CE<sub>1</sub> is low, CE<sub>2</sub> is high and OE is low for READ cycle.
- ADDRESS must be valid prior to, or coincident with CE<sub>1</sub> transition low and CE<sub>2</sub> transition high.

- Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

READ CYCLE NO. 2 (ADDRESS CONTROLLED) (5,6)

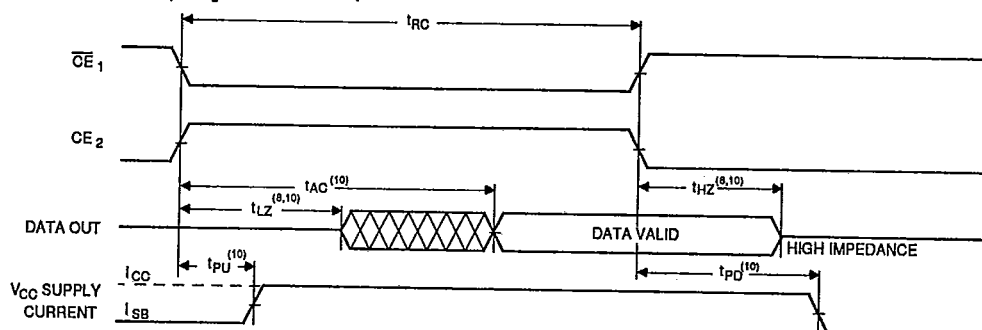
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1519 03

READ CYCLE NO. 3 ( $\overline{CE}_1$ ,  $CE_2$  CONTROLLED) (4,7,10)

2



1519 04

Notes:

9. READ Cycle Time is measured from the last valid address to the first transitioning address.

10. Transitions caused by a chip enable control have similar delays irrespective of whether  $\overline{CE}_1$  or  $CE_2$  causes them.



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# AC CHARACTERISTICS—WRITE CYCLE

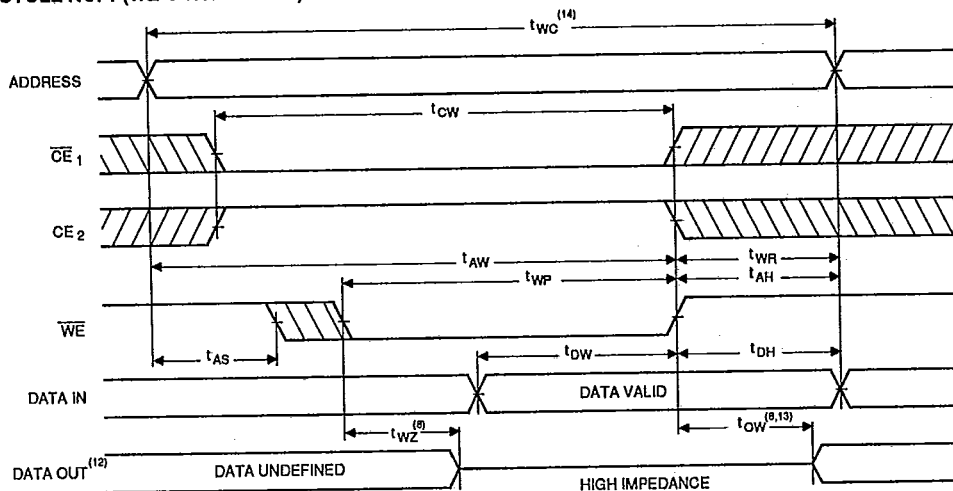
( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

| Sym.     | Parameter                        | -15* |     | -17 |     | -20 |     | -25 |     | -30 |     | -35 |     | -45 |     | Unit |
|----------|----------------------------------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|          |                                  | Min  | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| $t_{WC}$ | Write Cycle Time                 | 15   |     | 17  |     | 20  |     | 25  |     | 30  |     | 35  |     | 45  |     | ns   |
| $t_{CW}$ | Chip Enable Time to End of Write | 12   |     | 13  |     | 15  |     | 18  |     | 22  |     | 25  |     | 33  |     | ns   |
| $t_{AW}$ | Address Valid to End of Write    | 12   |     | 13  |     | 15  |     | 18  |     | 22  |     | 25  |     | 33  |     | ns   |
| $t_{AS}$ | Address Set-up Time              | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{WP}$ | Write Pulse Width                | 12   |     | 13  |     | 15  |     | 18  |     | 20  |     | 20  |     | 25  |     | ns   |
| $t_{AH}$ | Address Hold Time                | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{WR}$ | Write Recovery Time              | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{DW}$ | Data Valid to End of Write       | 9    |     | 10  |     | 11  |     | 13  |     | 15  |     | 15  |     | 20  |     | ns   |
| $t_{DH}$ | Data Hold Time                   | 0    |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{WZ}$ | Write Enable to Output in High Z |      | 7   |     | 7   |     | 8   |     | 10  |     | 12  |     | 14  |     | 18  | ns   |
| $t_{OW}$ | Output Active from End of Write  | 3    |     | 3   |     | 3   |     | 3   |     | 5   |     | 5   |     | 5   |     | ns   |

\* $V_{CC} = 5V \pm 5\%$  for -15

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## WRITE CYCLE NO. 1 (WE CONTROLLED)<sup>(11)</sup>



1519 05

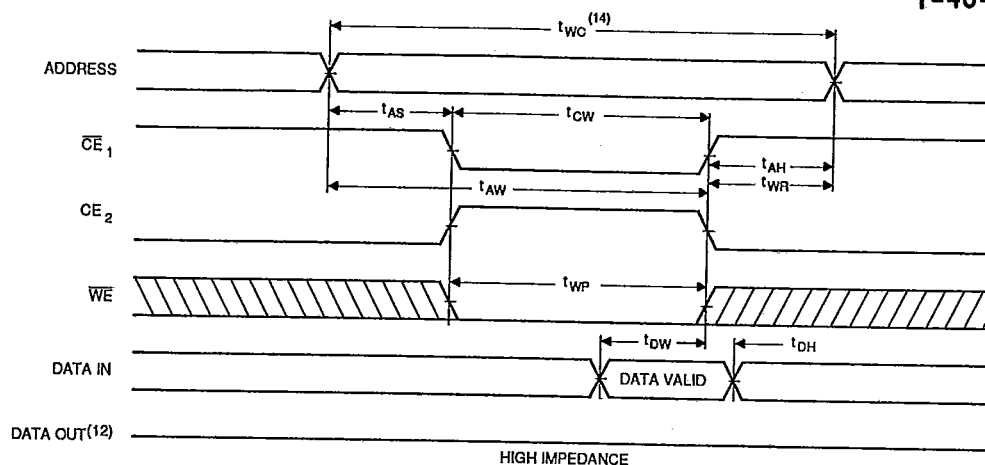
### Notes:

11.  $\overline{CE}_1$  and  $\overline{WE}$  must be low, and  $\overline{CE}_2$  high for WRITE cycle.
12.  $\overline{OE}$  is low for this WRITE cycle to show  $t_{WZ}$  and  $t_{OW}$ .
13. If  $\overline{CE}_1$  goes high, or  $\overline{CE}_2$  goes low, simultaneously with  $\overline{WE}$  high, the output remains in a low impedance state

14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE CONTROLLED) (11)

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AC TEST CONDITIONS

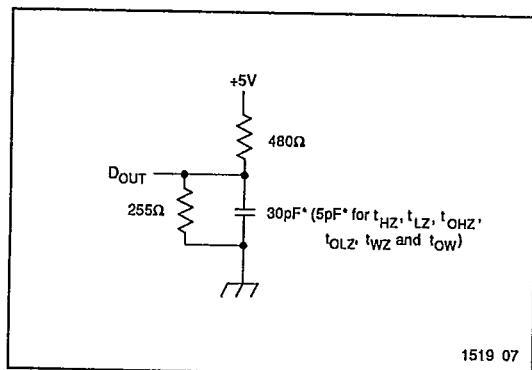
|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise and Fall Times     | 3ns                 |
| Input Timing Reference Level  | 1.5V                |
| Output Timing Reference Level | 1.5V                |
| Output Load                   | See Figures 1 and 2 |

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TRUTH TABLE

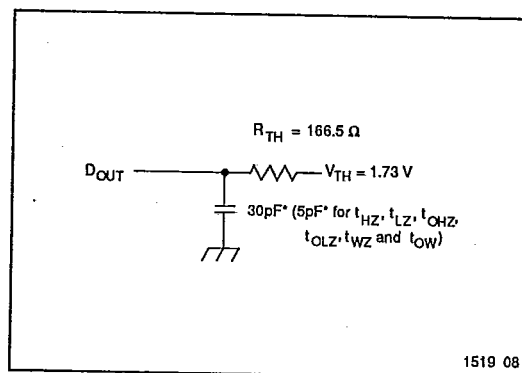
| Mode                      | CE <sub>1</sub> | CE <sub>2</sub> | OE | WE | I/O              | Power   |
|---------------------------|-----------------|-----------------|----|----|------------------|---------|
| Standby                   | H               | X               | X  | X  | High Z           | Standby |
| Standby                   | X               | L               | X  | X  | High Z           | Standby |
| D <sub>OUT</sub> Disabled | L               | H               | H  | H  | High Z           | Active  |
| Read                      | L               | H               | L  | H  | D <sub>OUT</sub> | Active  |
| Write                     | L               | H               | X  | L  | High Z           | Active  |

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Figure 1. Output Load



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Figure 2. Thevenin Equivalent

\* Including scope and test fixture.

Note:

Due to the ultra-high speed of the P4C164/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>cc</sub> and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V<sub>cc</sub> and ground. To

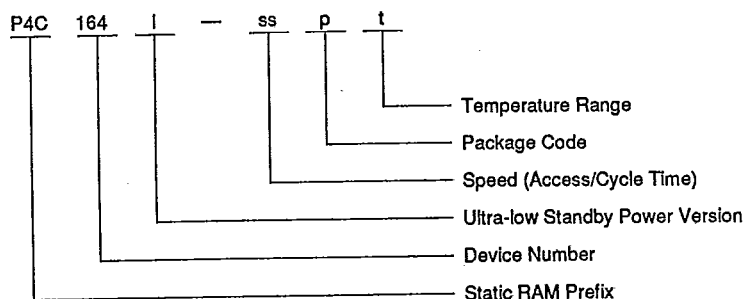
avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D<sub>OUT</sub> to match 166Ω (Thevenin Resistance).



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## ORDERING INFORMATION

The following part numbering scheme is used for



I = Ultra-low standby power designator L, if needed.  
ss = Speed (access/cycle time in ns), e.g., 25, 35  
p = Package code, i.e., P, J, C, DW, L.  
t = Temperature range, i.e., C, M, MB.

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### PACKAGE SUFFIX

| Package Suffix | Description                           |
|----------------|---------------------------------------|
| P              | Plastic DIP, 300 mil wide standard    |
| J              | Plastic SOJ, 300 mil wide standard    |
| C              | Sidebrazed DIP, 300 mil wide standard |
| DW             | CERDIP, 600 mil wide                  |
| L              | Leadless Chip Carrier (ceramic)       |

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### TEMPERATURE RANGE SUFFIX

| Temperature Range Suffix | Description                                     |
|--------------------------|-------------------------------------------------|
| C                        | Commercial Temperature Range, 0°C – +70°C.      |
| M                        | Military Temperature Range, –55°C – +125°C.     |
| MB                       | Mil. Temp. with MIL-STD-883C Class B compliance |

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### SELECTION GUIDE

The P4C164 is available in the following temperature, speed and package options. The P4C164L is only available with access times of 20ns and slower for commercial temperatures, 25ns and slower for military temperatures.

| Temp. Range      | Speed            | 15    | 17    | 20      | 25      | 30      | 35      | 45      |
|------------------|------------------|-------|-------|---------|---------|---------|---------|---------|
| Com'l            | Plastic DIP      | -15PC | -17PC | -20PC   | -25PC   | -30PC   | -35PC   | N/A     |
|                  | Plastic SOJ      | -15JC | -17JC | -20JC   | -25JC   | -30JC   | -35JC   | N/A     |
|                  | Sidebrazed DIP   | -15CC | -17CC | -20CC   | -25CC   | -30CC   | -35CC   | N/A     |
|                  | LCC              | -15LC | -17LC | -20LC   | -25LC   | -30LC   | -35LC   | N/A     |
| Mil. Temp.       | Sidebrazed DIP   | N/A   | N/A   | -20CM   | -25CM   | -30CM   | -35CM   | -45CM   |
|                  | CERDIP (600 mil) | N/A   | N/A   | -20DWM  | -25DWM  | -30DWM  | -35DWM  | -45DWM  |
|                  | LCC              | N/A   | N/A   | -20LM   | -25LM   | -30LM   | -35LM   | -45LM   |
| Military Proc'd* | Sidebrazed DIP   | N/A   | N/A   | -20CMB  | -25CMB  | -30CMB  | -35CMB  | -45CMB  |
|                  | CERDIP (600 mil) | N/A   | N/A   | -20DWMB | -25DWMB | -30DWMB | -35DWMB | -45DWMB |
|                  | LCC              | N/A   | N/A   | -20LMB  | -25LMB  | -30LMB  | -35LMB  | -45LMB  |

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\* Military temperature range with MIL-STD-883 Revision C, Class B processing.  
N/A = Not available

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