19-0111; Rev 0; 3/93

MAXIM

12-Bit Voltage-Output DACs with Reference

General Description

The MX667/MX767 are 12-bit digital-to-analog converters (DACs). Each includes a high-stability voltage reference, output amplifier, and input latches on a single IC.

The MX667 has a double-buffered input latch structure that is compatible with 4-,8-,12-, or 16-bit buses. The faster and simpler single-latch input structure of the MX767 is compatible with 12- and 16-bit buses. The MX667/MX767 latch responds to strobe pulses as short as 100ns and 40ns, respectively. Both the MX667 and the MX767 are designed for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. The MX667 is specified to ±1/4LSB maximum linearity error (K,B grades) at +25°C.

The precision high-speed output amplifier settles to within 1/2LSB for a 10V full-scale transition in 3.0µs.

Applications

Small Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Automatic Calibration
Machine and Motion Control Systems

Features

- **On-Chip Output Amplifier**
- **High-Stability Voltage Reference**
- **Guaranteed Monotonic Over Temperature**
- **Operate with ±12V or ±15V Supplies**
- **Very Fast Timing Specifications (40ns $\overline{CS}$ pulse width, MX767 only)**
- **Low 144mW Power Dissipation**
- **All Timing Specifications Guaranteed Over Temperature**

Ordering Information

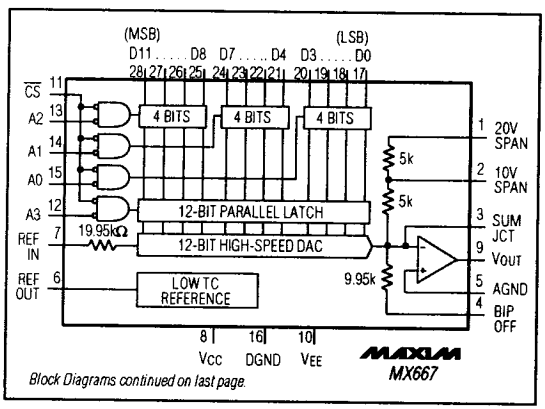
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MX667JN	0°C to +70°C	28 Plastic DIP	±1/2
MX667KN	0°C to +70°C	28 Plastic DIP	±1/4
MX667JCWI	0°C to +70°C	28 SO	±1/2
MX667KCWI	0°C to +70°C	28 SO	±1/4
MX667JP	0°C to +70°C	28 PLCC	±1/2
MX667KP	0°C to +70°C	28 PLCC	±1/4

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C.*

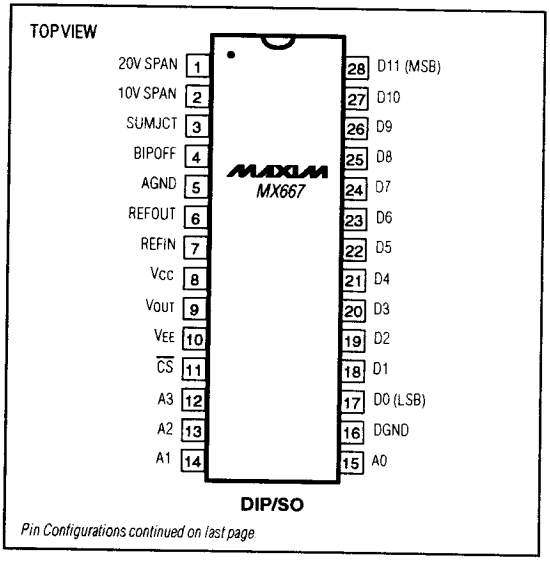
***Contact factory for availability and processing to MIL-STD-883.*

Block Diagrams



Block Diagrams continued on last page.

Pin Configurations



Pin Configurations continued on last page.

12-Bit Voltage-Output DACs with Reference

ABSOLUTE MAXIMUM RATINGS

VCC to DGND ..... -0.3V, +18V
VEE to DGND ..... +0.3V, -18V
Digital Input Voltage to DGND ..... -0.3V, VCC + 0.3V
REF IN to AGND ..... ±12V
BIP OFF to AGND ..... ±12V
10V SPAN to AGND ..... ±12V
20V SPAN to AGND ..... ±24V
REF OUT (Note 1) ..... Continuous Short to AGND or VCC
VOUT (Note 1) ..... Continuous Short to VEE or VCC

Continuous Power Dissipation (TA = +70°C)
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1067mW
24-Pin SO (derate 11.76mW/°C above +70°C) 941mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin Plastic DIP (derate 14.29mW/°C above +70°C) . 1143mW
28-Pin SO (derate 12.50mW/°C above +70°C) 1000mW
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
28-Pin LCC (derate 10.20mW/°C above +70°C) 816mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C) . 1333mW
Operating Temperature Ranges:
MX_67J_/K_/JC_/KC_ ..... 0°C to +70°C
MX_67A_/B_/JE__/KE_ ..... -40°C to +85°C
MX_67S_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: VOUT may be shorted to AGND, VCC, or VEE if the package power dissipation is not exceeded. REFOUT may be shorted to AGND or VCC if the package power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC and VEE = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, RL = 2kΩ, CL = 500pF, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 2)							
Resolution				12			Bits
Integral Nonlinearity	INL	TA = +25°C	MX667K/B			±1/4	LSB
			MX667J/A/S			±1/2	
		TA = TMIN to TMAX	MX667K/B			±1/2	
			MX667J/A/S			±3/4	
		TA = +25°C	MX767K/B			±1/2	
			MX767J/A/S			±1	
		TA = TMIN to TMAX	MX767K/B			±1/2	
			MX767J/A/S			±1	
Differential Nonlinearity	DNL	TA = +25°C	MX667K/B			±1/2	LSB
			MX667J/A/S			±3/4	
		TA = TMIN to TMAX	MX667 all grades			±1	
		TA = TMIN to TMAX	MX767 all grades			±1	
Gain Error						±0.2	%FSR
Unipolar Offset Error		BIPOFF = AGND				±2	LSB
Bipolar Offset Error		(Note 3)				±0.1	%FSR
DIGITAL INPUTS							
Input Voltage High	VIH	TA = TMIN to TMAX		2.0			V
Input Voltage Low	VIL	TA = TMIN to TMAX				0.8	V
Input Current High	IIH	All control inputs, D0-D11, VIH = 5.5V				±10	µA
Input Current Low	IIL	All control inputs, D0-D11, VIL = 0.8V				±5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} and V_{EE} = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIFT							
Differential Nonlinearity	DNL				±2		ppm FSR/°C
Gain Error		$T_A = T_{MIN}$ to T_{MAX}	MX_67K/B			±15	ppm FSR/°C
			MX_67J/A/S			±30	
Unipolar Offset Error		$T_A = T_{MIN}$ to T_{MAX}				±3	ppm FSR/°C
Bipolar Offset Error		$T_A = T_{MIN}$ to T_{MAX}				±10	ppm FSR/°C
CONVERSION SPEED							
Settling Time to 0.01% FSR		10kΩ feedback resistor (20V swing)			3	4	µs
		5kΩ feedback resistor (10V swing)			2	3	
		For 1LSB change			1		
Slew Rate				10	15		V/µs
ANALOG OUTPUT							
Output Current		$(V_{EE} + 2.5V) \le V_{OUT} \le (V_{CC} - 2.5V)$				±5	mA
Output Impedance					0.05		Ω
Short-Circuit Current					±40		mA
REFERENCE OUTPUT							
Output Voltage				9.95		10.05	V
Maximum External Current (exclusive of BIPOFF and REFIN)				2			mA
POWER-SUPPLY SENSITIVITY							
Positive Supply Rejection (Note 4)		V_{CC} = 11.4V to 16.5V			5	10	ppm FSR/%
Negative Supply Rejection (Note 4)		V_{EE} = -11.4V to -16.5V			5	10	ppm FSR/%
POWER-SUPPLY REQUIREMENTS							
Supply Current	I_{CC}	V_{CC} = 16.5V, code set for worst-case I_{CC}			8	12	mA
	I_{EE}	V_{EE} = -16.5V, code set for worst-case I_{EE}			4	8	

Note 2: Accuracy specifications are tested with a 50Ω resistor between the REFIN and REFOUT pins (as shown in Table 3, Figure 5, and Figure 6).
Note 3: Tested with a 50Ω resistor between REFOUT and BIPOFF.
Note 4: A minimum supply of ±12.5V is required for a ±10V output range.

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TIMING CHARACTERISTICS - MX667

(V_{CC} and V_{EE} = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, R_L = 2kΩ, C_L = 500pF, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid to End of $\overline{CS}$	t_{DC}	$T_A = T_{MIN}$ to T_{MAX}	50	40		ns
Address Valid to End of $\overline{CS}$	t_{AC}	$T_A = T_{MIN}$ to T_{MAX}	100	45		ns
$\overline{CS}$ Pulse Width	t_{CP}	$T_A = T_{MIN}$ to T_{MAX}	100	45		ns
Data-Hold Time	t_{DH}	$T_A = T_{MIN}$ to T_{MAX}	0	-5		ns
Address-Hold Time	t_{AH}	$T_A = T_{MIN}$ to T_{MAX}	0	-5		ns

12-Bit Voltage-Output DACs with Reference

TIMING CHARACTERISTICS - MX767

(VCC and VEE = ±12V or ±15V, DGND = AGND = 0V, REFIN = REFOUT, RL = 2kΩ, CL = 500pF, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Valid to End of $\overline{CS}$	tDC	TA = +25°C	All grades	40	30		ns
		TA = TMIN to TMAX	MX767J/K/A/B	60	35		
			MX767S	90	40		
$\overline{CS}$ Pulse Width	tCP	TA = +25°C	All grades	40	30		ns
		TA = TMIN to TMAX	MX767J/K/A/B	60	35		
			MX767S	90	40		
Data-Hold Time	tDH	TA = +25°C	All grades	10	0		ns
		TA = TMIN to TMAX	MX767J/K/A/B	10	0		
			MX767S	20	0		

Note 2: Accuracy specifications are tested with a 50Ω resistor between the REFIN and REFOUT pins (as shown in Table 3, Figure 5, and Figure 6).

Pin Description

PIN			NAME	FUNCTION
MX667	MX767			
All	DIP/SO	PLCC		
1	1	2	20V SPAN	Application Resistor for 20V output
2	2	3	10V SPAN	Application Resistor for 10V output
3	3	4	SUMJCT	Summing Junction
4	4	5	BIPOFF	Bipolar Offset Resistor
5	5	6	AGND	Analog Ground
6	6	7	REFOUT	10V Reference Output
7	7	9	REFIN	Reference Input
8	8	10	VCC	Positive Supply
9	9	11	VOUT	Amplifier Output
10	10	12	VEE	Negative Supply
11	11	13	$\overline{CS}$	Chip Select
12-15	–	–	A3-A0	Address Selects
16	12	14	DGND	Digital Ground
17-28	13-24	16-21, 23-28	D0-D11	Data Bits 0 through 11
–	–	1, 8, 15, 22	N.C.	No Connect - not internally connected

Table 1. MX667 Operation

$\overline{CS}$	A3	A2	A1	A0	OPERATION
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

1 = High State, 0 = Low State, X = Don't Care

Table 2. MX767 Operation

$\overline{CS}$	OPERATION
1	No Operation
0	Input Register is Transparent
R	Input Register is Latched

1 = High State, 0 = Low State, R = Rising Edge

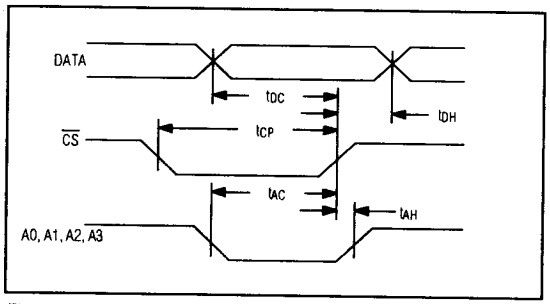


Figure 1. MX667 Timing

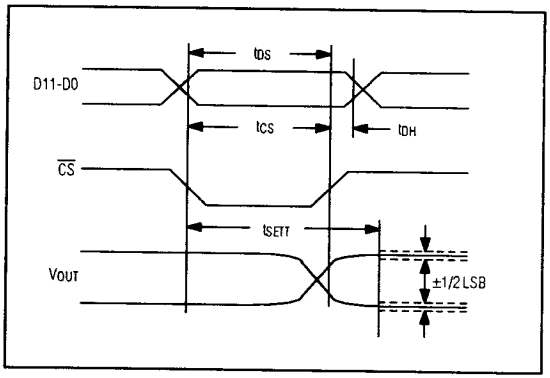


Figure 2. MX767 Timing

Detailed Description

Digital Inputs and Interface Logic

The MX667/MX767 digital inputs are compatible with both TTL and 5V CMOS logic. Supply current is specified for TTL input levels (worst case), but is reduced (by about 1mA) when the data inputs are low.

Table 1 shows the truth table for the MX667 control inputs; Table 2 shows the truth table for the MX767. Figures 1 and 2 illustrate the digital timing for the MX667 and MX767.

Input Coding

Unipolar coding is straight binary, where all zeros (000H) on the data inputs yield a zero analog output and all ones (FFFH) yield an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000H yields a minus full-scale output, an input of FFFH yields an output 1LSB below positive full scale, and zero occurs for an input code of 800H.

The MX667/MX767 can be used with twos-complement input coding if an inverter is used on the most significant bit (MSB, D11).

Double-Buffered Latches (MX667)

The MX667's bus interface logic consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers that can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 3 shows the MX667 logic section block diagram.

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input, all of which are active low. The four address lines each enable one of the four latches, as indicated in Table 2.

All latches in the MX667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. The data is latched when any one of the control signals returns high.

It is permissible to enable more than one of the latches simultaneously. If a first-rank latch is enabled coincident with the second-rank latch, the data will reach the second rank correctly if the write-cycle timing specifications are met for both the first- and second-rank latches.

12-Bit Voltage-Output DACs with Reference

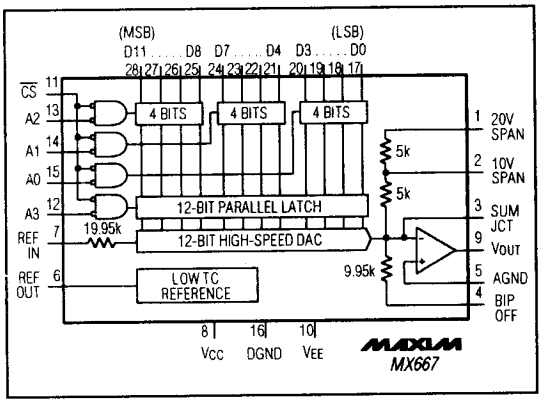


Figure 3. MX667 Block Diagram

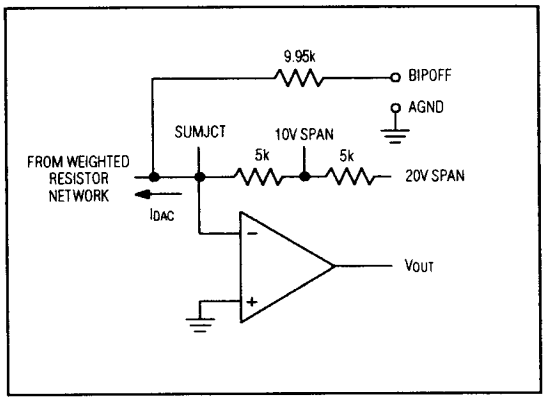


Figure 4. Output Amplifier Voltage Range Scaling Circuit

Table 3. Output Voltage Range Connections

Output Range (V)	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10	Offset Binary	1	9	N.C.	6 (through 50Ω fixed or 100Ω trim resistor)
±5	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ω trim resistor)
±2.5	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ω trim resistor)
0 to +10	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – see Figure 5)
0 to +5	Straight Binary	2	3	9	5 (or optional trim – see Figure 5)

Note: Pin numbers apply to DIP/SO packages.

Output Buffer Amplifier

The output amplifier is an inverting amplifier that can be configured for several gain settings (Figure 4). The output can also be "level shifted" from AGND by using BIPOFF as a bipolar offset resistor. The output buffer amplifier is capable of driving a 2kΩ resistor in parallel with a 500pF capacitor.

The output amplifier's small-signal bandwidth is typically 5MHz. The amplifier's output noise is approximately 15nV/√Hz at a frequency of 1kHz. The amplifier's output broadband noise is approximately 25μVRMS, and is not strongly power-supply-voltage dependent.

Voltage Reference

The MX667/MX767 have an internal low-noise reference that is trimmed for absolute accuracy and temperature coefficient. Performance is specified with the internal reference driving the DAC, since all trimming and testing are done in this configuration.

In addition to the reference currents required for the DAC (typically 0.5mA to REFIN and 1.0mA to BIPOFF), the internal reference has sufficient buffering to drive external circuitry. A minimum of 0.1mA is available for driving external loads.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a ±1% tolerance, and the MX667/MX767 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the MX667/MX767 when used with the internal reference.

External references other than 10V may be used. The recommended range of reference voltage is from +8V to +10.5V, which allows both 8.192V and 10.24V ranges to be used.

External feedback resistors should not be used to modify the scale factor of the MX667/MX767. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip.

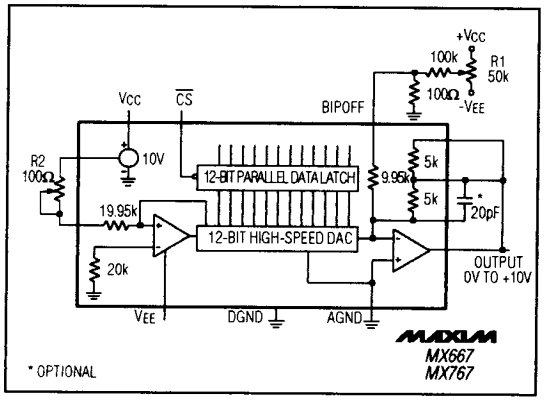


Figure 5. 0V to +10V Unipolar Voltage Output

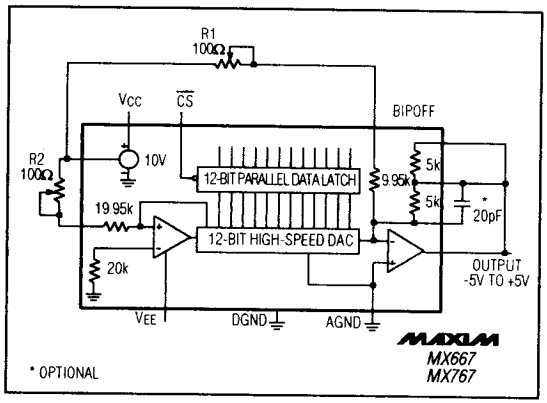


Figure 6. ±5V Bipolar Voltage Output

Applications Information

Offset and Gain Adjust, Unipolar Mode

Figure 5 configuration provides a unipolar 0V to +10V output range. In this mode, BIPOFF should be grounded if not used for trimming.

STEP 1. ZERO ADJUST
Turn all bits OFF and adjust zero trimmer R1 until the output reads 0.000V (1LSB = 2.44mV). In most cases this trim is not needed, and BIPOFF should be connected to AGND.

STEP 2. GAIN ADJUST
Turn all bits on and adjust the 100Ω gain trimmer, R2, until the output is 9.9976V. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000V.)

Offset and Gain Adjust, Bipolar Mode

Figure 6 configuration provides a bipolar output voltage from -5.000V to +4.9976V, with positive full scale occurring with all bits on (all 1s).

STEP 1. OFFSET ADJUST
Turn all bits off. Adjust the 100Ω trimmer, R1, to give a -5.000V output.

STEP 2. GAIN ADJUST
Turn all bits on. Adjust the 100Ω gain trimmer, R2, to give a reading of +4.9976V.

STEP 3. BIPOLAR ZERO ADJUST (Optional)
In applications where an accurate zero output is required, set the MSB on, all other bits off, and readjust R1 for a 0V output.

Power-Supply Decoupling and Ground Management

The MX667/MX767 have separate analog and digital grounds to provide optimum connections for low-noise and high-speed performance. These grounds should be tied together at the system power ground.

AGND is the ground point for the output amplifier, DAC, and reference, and is thus the "high-quality" ground for the MX667/MX767; it should be connected directly to the system's analog reference point. DGND should be returned separately to the system power ground. High-frequency noise on DGND may feed through to the converter output; for optimum performance, DGND noise should be kept well below 200mV.

Connect a decoupling capacitor 0.1µF I I 10µF from each power-supply pin (VCC and VEE) to AGND. Any load driven by the output amplifier should also be referred to AGND.

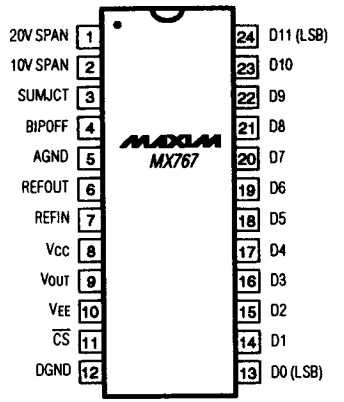
Digital Input Considerations

The threshold of the digital-input circuitry is set at 1.4V and does not change significantly with supply voltage. Thus, the MX667/MX767 digital interface may be driven with any of the popular types of 5V logic.

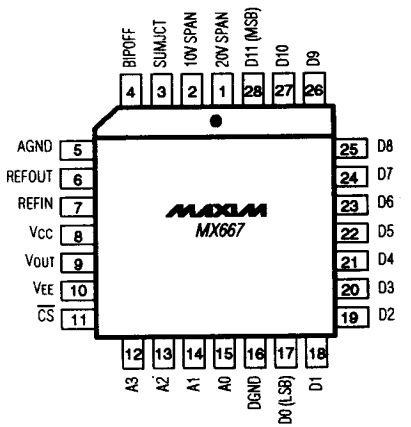
12-Bit Voltage-Output DACs with Reference

Pin Configurations (continued)

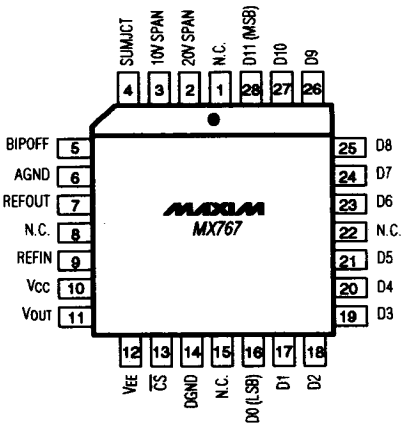
TOP VIEW



DIP/SO

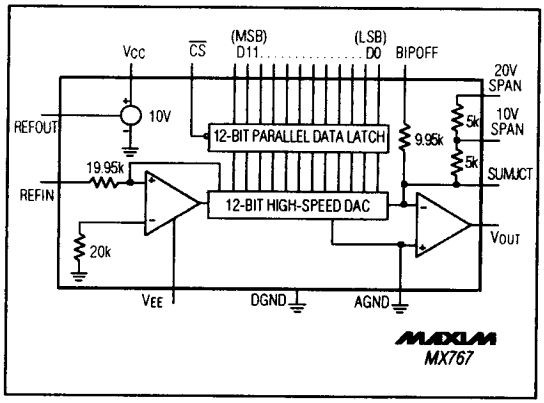


PLCC/LCC



PLCC

Block Diagrams (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MX667C/D	0°C to +70°C	Dice*	±1/2
MX667JEPI	-40°C to +85°C	28 Plastic DIP	±1/2
MX667KEPI	-40°C to +85°C	28 Plastic DIP	±1/4
MX667JEWI	-40°C to +85°C	28 SO	±1/2
MX667KEWI	-40°C to +85°C	28 SO	±1/4
MX667JEQI	-40°C to +85°C	28 PLCC	±1/2
MX667KEQI	-40°C to +85°C	28 PLCC	±1/4
MX667AD	-40°C to +85°C	28 CERDIP	±1/2
MX667BD	-40°C to +85°C	28 CERDIP	±1/4
MX667SE	-55°C to +125°C	28 LCC**	±1/2
MX667SD	-55°C to +125°C	28 CERDIP**	±1/2
MX767JN	0°C to +70°C	24 Narrow Plastic DIP	±1
MX767KN	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MX767JCWG	0°C to +70°C	24 SO	±1
MX767KCWG	0°C to +70°C	24 SO	±1/2
MX767JP	0°C to +70°C	28 PLCC	±1
MX767KP	0°C to +70°C	28 PLCC	±1/2
MX767C/D	0°C to +70°C	Dice*	±1
MX767JENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MX767KENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MX767JEWG	-40°C to +85°C	24 SO	±1
MX767KEWG	-40°C to +85°C	24 SO	±1/2
MX767JEQI	-40°C to +85°C	28 PLCC	±1
MX767KEQI	-40°C to +85°C	28 PLCC	±1/2
MX767AD	-40°C to +85°C	24 Narrow CERDIP	±1
MX767BD	-40°C to +85°C	24 Narrow CERDIP	±1/2
MX767SD	-55°C to +125°C	24 Narrow CERDIP	±1

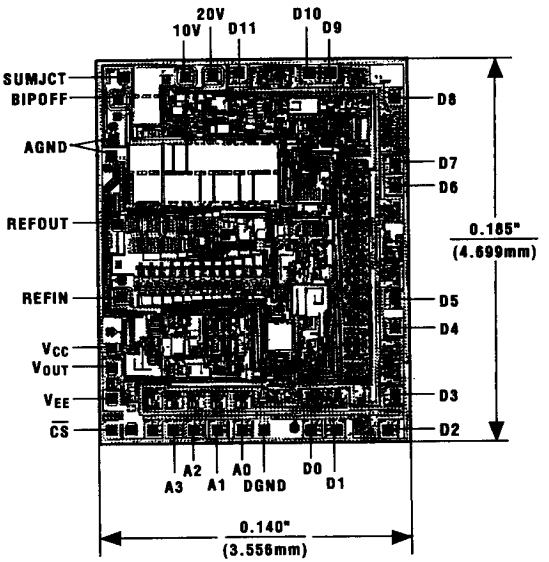
** Dice are tested at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

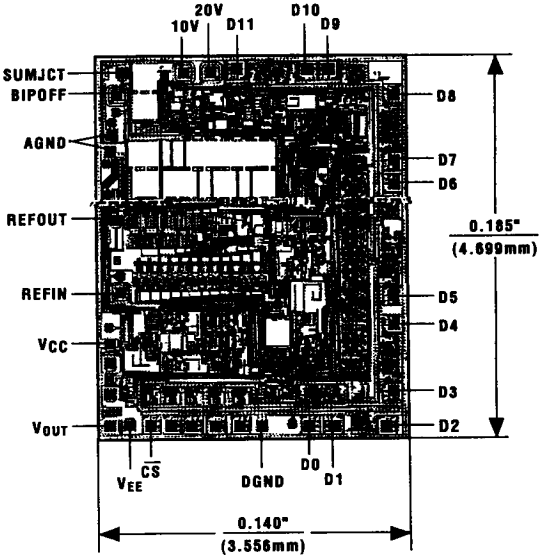
12-Bit Voltage-Output DACs with Reference

Chip Topographies

MX667



MX767



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