

PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}, V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved

40A

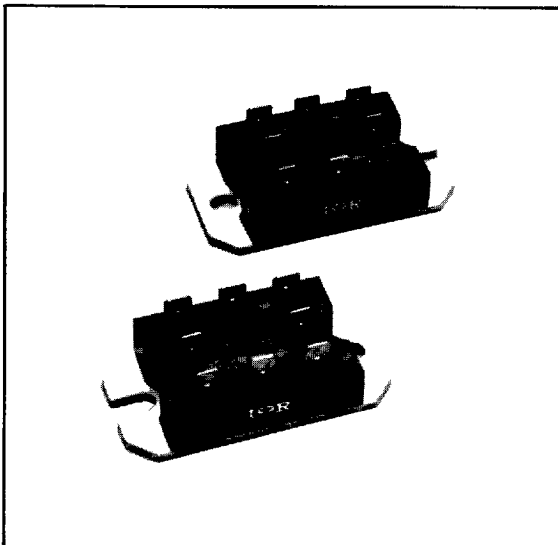
Description

The P400 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

Major Ratings and Characteristics

Parameters	P400	Units
I_D	40	A
@ T_C	85	°C
I_{FSM} @ 50Hz	385	A
@ 60Hz	400	A
I^2t @ 50Hz	745	A ² s
@ 60Hz	680	A ² s
I^2/t	7450	A ² /s
V _{RRM} range	400 to 1200	V
V _{INS}	2500	V
T _J	-40 to 125	°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	V_{RRM} maximum repetitive peak reverse voltage V	V_{RSM} maximum non-repetitive peak reverse voltage V	V_{DRM} maximum repetitive peak off-state voltage V
P401, P411, P421, P431, P441, P461, P471	400	500	400
P402, P412, P422, P432, P442, P462, P472	600	700	600
P403, P413, P423, P433, P443, P463, P473	800	900	800
P404, P414, P424, P434, P444, P464, P474	1000	1100	1000
P405, P415, P425, P435, P445, P465, P475	1200	1300	1200

On-state Conduction

Parameters	P400	Units	Conditions
I_D Maximum DC output Current	40	A	@ $T_C = 85^\circ\text{C}$, full bridge circuits 0,1,2 and 3
$I_{T(AV)}$ $I_{F(AV)}$ Maximum average on-state and forward current	20	A	180° sine conduction circuits 6, 7
I_{RMS} Maximum RMS current	44	A	180° sine conduction circuit 4
I_{TSM} Maximum peak one-cycle non repetitive on-state or forward current I_{FSM}	385	A	10ms
	400	A	8.3ms
	325	A	10ms
	340	A	8.3ms
i^2t Maximum i^2t for fusing	745	A ² s	10ms
	680	A ² s	8.3ms
	530	A ² s	10ms
	480	A ² s	8.3ms
i^2/t Maximum i^2/t for fusing	7450	A ² /s	t=0 to 10ms, no voltage reapplied i^2t for time tx = $i^2/t \cdot tx$
$V_{T(TO)}$ Maximum value of threshold voltage	0.85	V	$T_J = 125^\circ\text{C}$
r_t Maximum value of on-state or forward slope resistance	7.89	mΩ	$T_J = 125^\circ\text{C}$, Av. power = $V_{T(TO)} \cdot I_{T(AV)} + r_t \cdot (I_{T(RSM)})^2$
V_{TM} Maximum peak on-state or forward voltage drop V_{FM}	1.35	V	$T_J = 25^\circ\text{C}$ $I_{TM} = \pi \times I_{T(AV)}$
	1.35	V	$T_J = 25^\circ\text{C}$ $I_{FM} = \pi \times I_{F(AV)}$
di/dt Maximum non repetitive rate of rise of turned on current	200	A/μs	$T_J = 125^\circ\text{C}$ from 0.67 V_{DRM} $I_{TM} = \pi \times I_{T(AV)}$, $I_G = 500\text{mA}$, $tr < 0.5 \mu\text{s}$, $tp > 6 \mu\text{s}$
I_H Maximum holding current	100	mA	$T_J = 25^\circ\text{C}$ anode supply=6V, resistive load, gate open
I_L Maximum latching current	250	mA	$T_J = 25^\circ\text{C}$ anode supply=6V, resistive load.

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Blocking

Parameters	P400	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	200	V/ μ s	$T_J=125^\circ\text{C}$, exponential to $0.67 V_{\text{DRM}}$ gate open
I_{RRM} Maximum peak reverse and off-state leakage current at $V_{\text{RRM}}, V_{\text{DRM}}$	10	mA	$T_J=125^\circ\text{C}$, gate open circuit
I_{RRM} Max. peak reverse leakage current	100	μ A	$T_J = 25^\circ\text{C}$
V_{INS} RMS isolation voltage	2500	V	50Hz, circuit to base, all terminals shorted $T_J = 25^\circ\text{C}$, $t = 1 \text{ s}$

Triggering

Parameters	P400	Units	Conditions
P_{GM} Maximum peak gate power	8.0	W	
$P_{\text{G(AV)}}$ Maximum average gate power	2.0	W	
I_{GM} Maximum peak gate current	2.0	A	
$-V_{\text{GM}}$ Maximum peak negative gate voltage	10	V	
V_{GT} Maximum gate voltage required to trigger	3.0	V	$T_J=-40^\circ\text{C}$
	2.0	V	$T_J = 25^\circ\text{C}$
	1.0	V	$T_J=125^\circ\text{C}$
I_{GT} Maximum gate current required to trigger	90	mA	$T_J = -40^\circ\text{C}$
	60	mA	$T_J = 25^\circ\text{C}$
	35	mA	$T_J=125^\circ\text{C}$
V_{GD} Maximum gate voltage that will not trigger	0.2	V	$T_J=125^\circ\text{C}$, rated V_{DRM} applied
I_{GD} Maximum gate current that will not trigger	2.0	mA	$T_J=125^\circ\text{C}$, rated V_{DRM} applied

Thermal and Mechanical Specifications

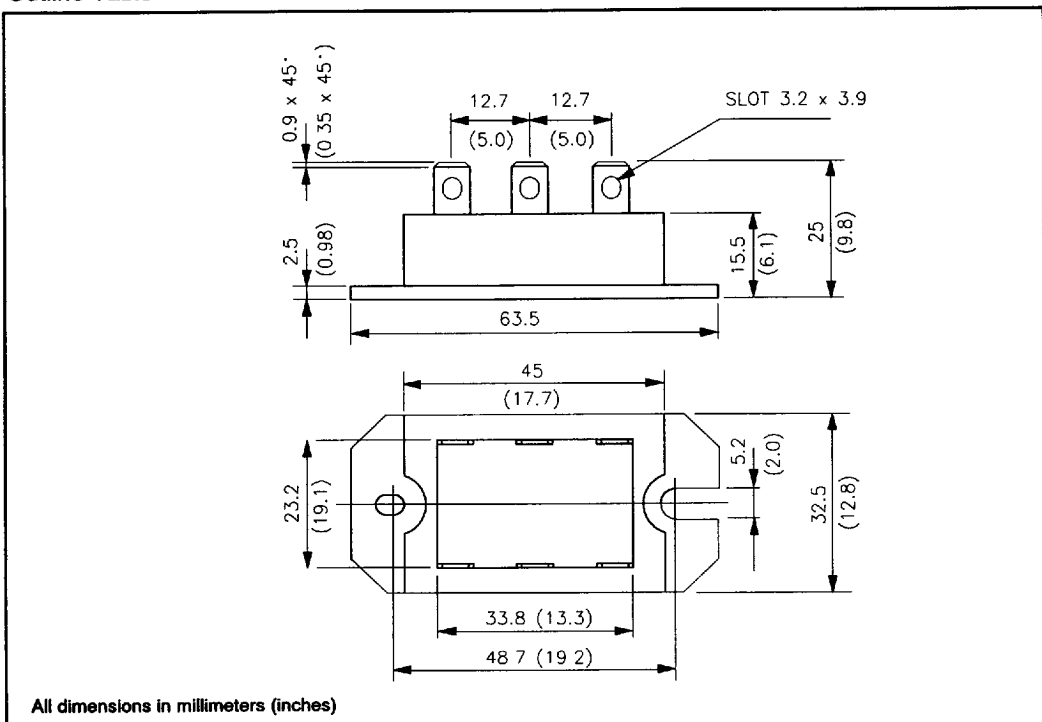
Parameters	P400	Units	Conditions
T_J Junction temperature range	-40 to 125	$^\circ\text{C}$	
T_{stg} Storage temperature range	-40 to 150	$^\circ\text{C}$	
R_{thJC} Maximum thermal resistance, junction to case	1.05	K/W	DC operation per junction
R_{thCS} Maximum thermal resistance	0.10	K/W	Mounting surface smooth and greased per module 0,1,2,3
	0.20	K/W	Mounting surface smooth and greased per module 4,6,7
T Mounting torque, base to heatsink $\pm 10\%$	5	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound.
wt Approximate weight	58 (2.0)	g (oz)	

Circuit Type and Coding *

	Circuit*0"	Circuit*1"	Circuit*2"	Circuit*3"	Circuit*4"	Circuit*6"	Circuit*7"
Terminal Positions							
Schematic diagram							
	Single Phase Hybrid Bridge Common Cathode	Single Phase Hybrid Bridge Common Anode	Single Phase Hybrid Bridge Doubler Connection	Single Phase All SCR Bridge	SCR AC Switch	Hybrid Doubler	SCR Doubler
Basic series	P40.	P41.	P42.	P43.	P44.	P46.	P47.
With voltage suppression	P40.K	P41.K	P42.K	P43.K	P44.K	-	-
With free-wheeling diode	P40.W	41.W	-	-	-	-	-
With both voltage suppression and free-wheeling diode	P40.KW	P41.KW	-	-	-	-	-

* To complete code refer to voltage ratings table, i.e.: for 600V P410.W complete code is P402W

Outline Table



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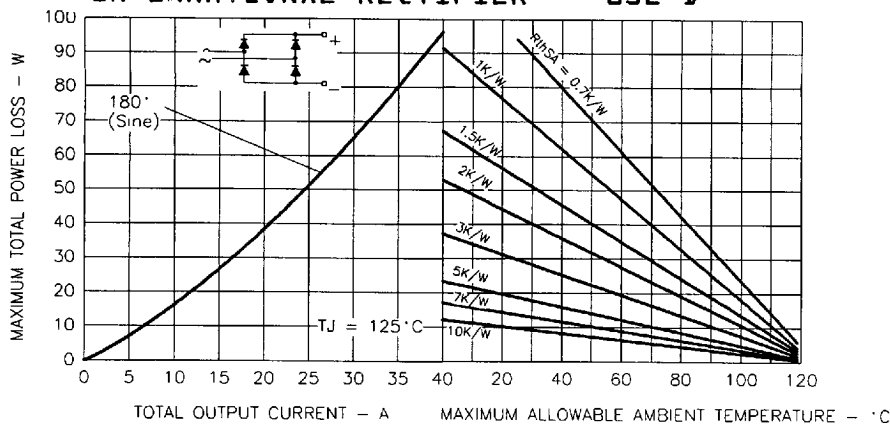


Fig. 1 - Current Rating Nomogram (1 Module Per Heatsink), Circuits '0', '1', '2', '3'

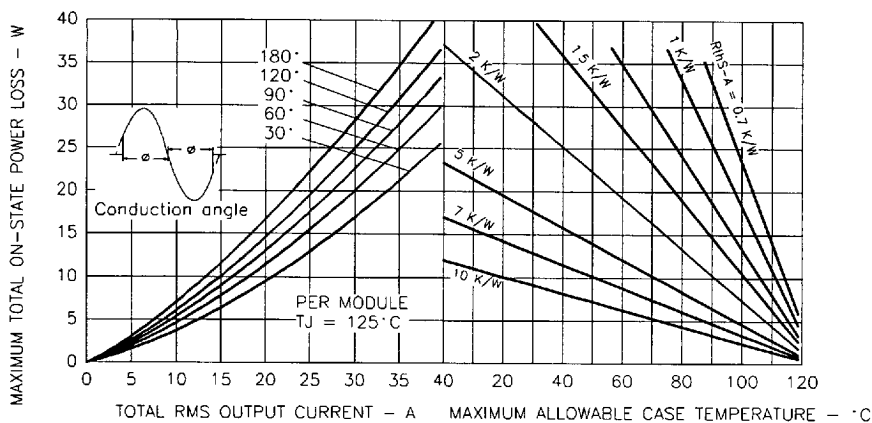


Fig. 2 - Current Rating Nomogram (1 Module Per Heatsink), Circuit '4'

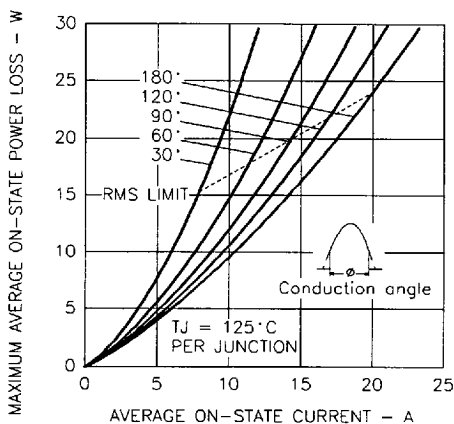


Fig. 3 - On-state Power Loss Characteristics

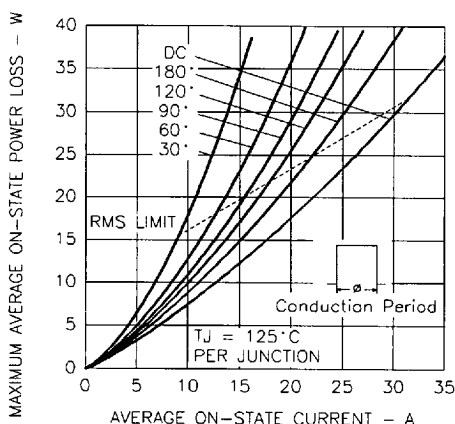


Fig. 4 - On-state Power Loss Characteristics

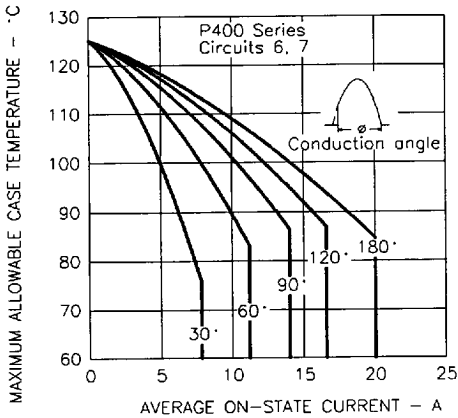


Fig. 5 - Current Ratings Characteristics

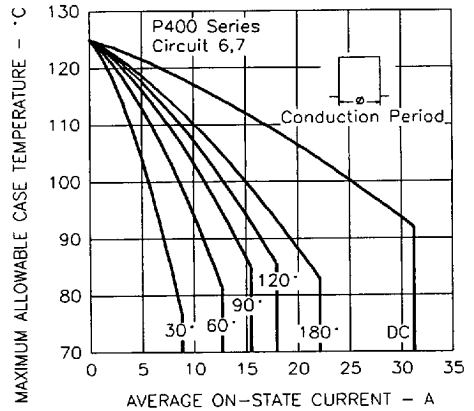


Fig. 6 - Current Ratings Characteristics

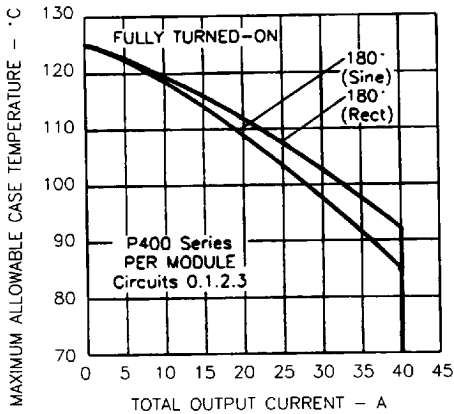


Fig. 7 - Current Ratings Characteristics

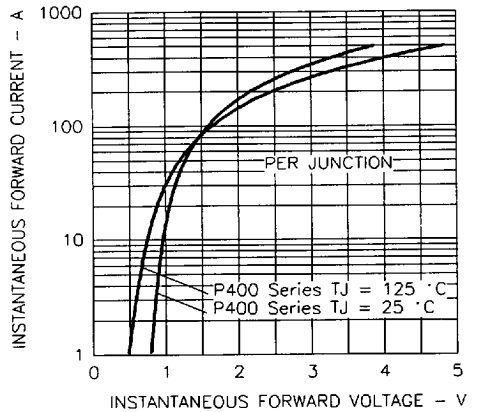


Fig. 8 - On-state Voltage Drop Characteristics

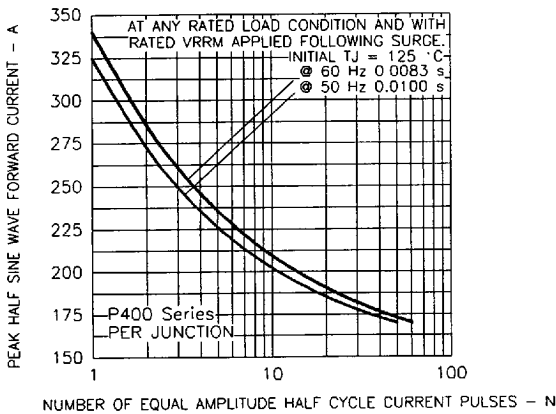


Fig. 9 - Maximum Non-Repetitive Surge Current

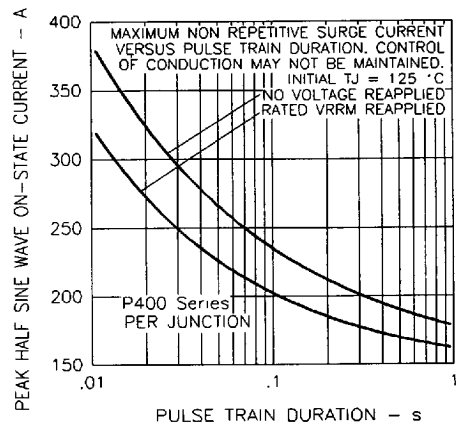


Fig. 10 - Maximum Non-Repetitive Surge Current

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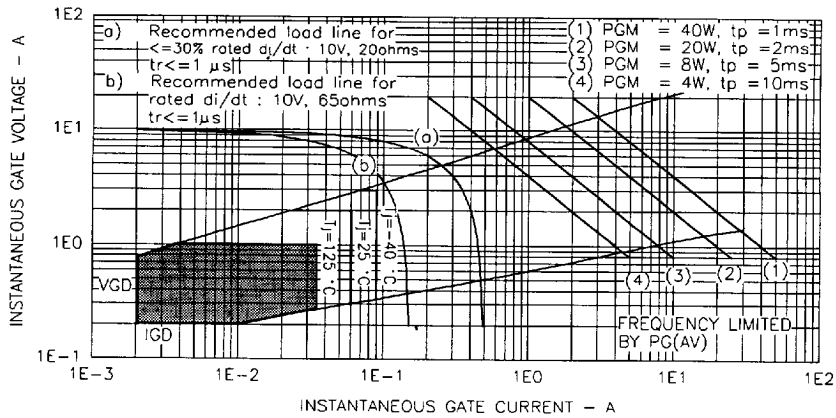


Fig. 11 - Gate Characteristics

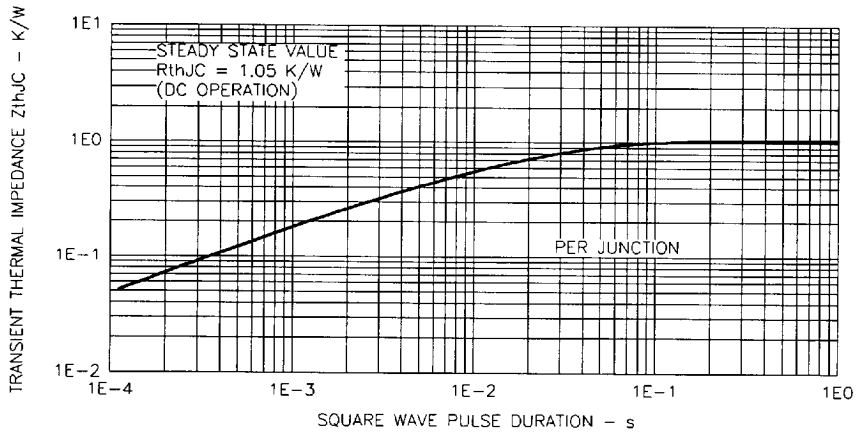


Fig. 12 - Thermal Impedance Z_{thJC} Characteristics