



Not Intended For New Designs

T-45-07

100180 High-Speed 6-Bit Adder

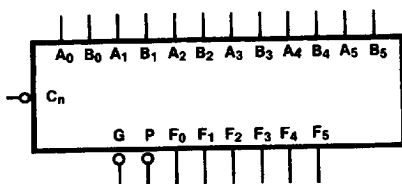
General Description

The 100180 is a high-speed 6-bit adder capable of performing a full 6-bit addition of two operands. Inputs for the adder are active-LOW Carry, Operand A, and Operand B; outputs are Function, active-LOW Carry Generate, and ac-

tive-LOW Carry Propagate. When used with the 100179 Full Carry Lookahead as a second order lookahead block, the 100180 provides high-speed addition of very long words. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

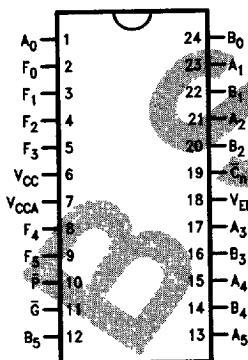


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Pin Names	Description
A ₀ -A ₅	Operand A Inputs
B ₀ -B ₅	Operand B Inputs
C _n	Carry Input (Active LOW)
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)
F ₀ -F ₅	Function Outputs

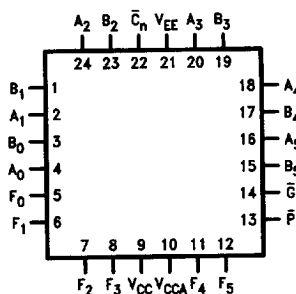
Connection Diagrams

24-Pin DIP



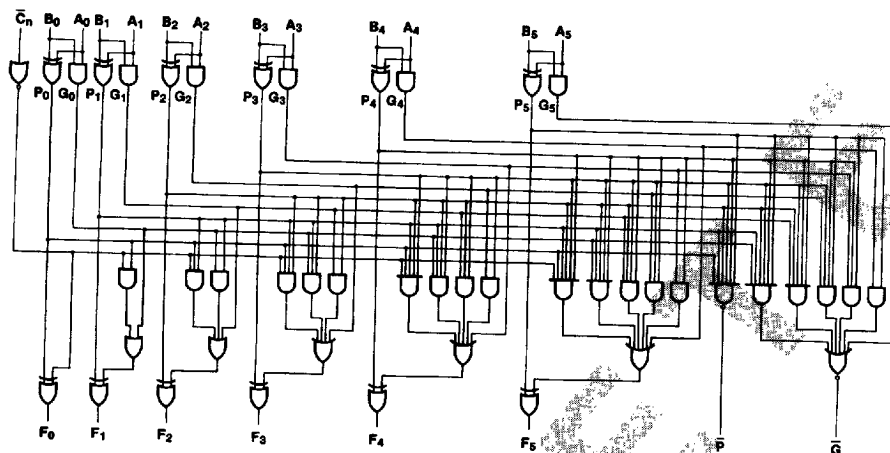
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24-Pin Quad Cerpak



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Logic Diagram



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Logic Equations

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$i = 0, 1, 2, 3, 4, 5$$

$$F_0 = P_0 \oplus C_n$$

$$F_1 = P_1 \oplus (G_0 + P_0 C_n)$$

$$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_n)$$

$$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n)$$

$$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n)$$

$$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_n)$$

$$\bar{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$$

$$\bar{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C

Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C)

0°C to +85°C

V_{EE} Pin Potential to Ground Pin

-7.0V to +0.5V

Input Voltage (DC)

V_{EE} to +0.5V

Output Current (DC Output HIGH)

-50 mA

Operating Range (Note 2)

-5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1025	-955	-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810	-1705	-1620			
V _{OHC}	Output HIGH Voltage	-1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1020		-870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810		-1605			
V _{OHC}	Output HIGH Voltage	-1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1595			
V _{IH}	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1035		-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1830		-1620			
V _{OHC}	Output HIGH Voltage	-1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			220	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-290	-195	-135	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.70	1.10	4.60	1.10	4.70	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\bar{F}$	1.00	3.00	1.00	3.00	1.00	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\bar{G}$	1.40	3.90	1.40	3.80	1.40	3.90	ns	
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_n$ to F_n	1.10	4.00	1.10	3.90	1.10	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.40	ns	

Cerpack AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.50	1.10	4.40	1.10	4.50	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\bar{F}$	1.00	2.80	1.00	2.80	1.00	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\bar{G}$	1.40	3.70	1.40	3.60	1.40	3.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_n$ to F_n	1.10	3.80	1.10	3.70	1.10	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.30	0.45	2.20	0.45	2.30	ns	

100180

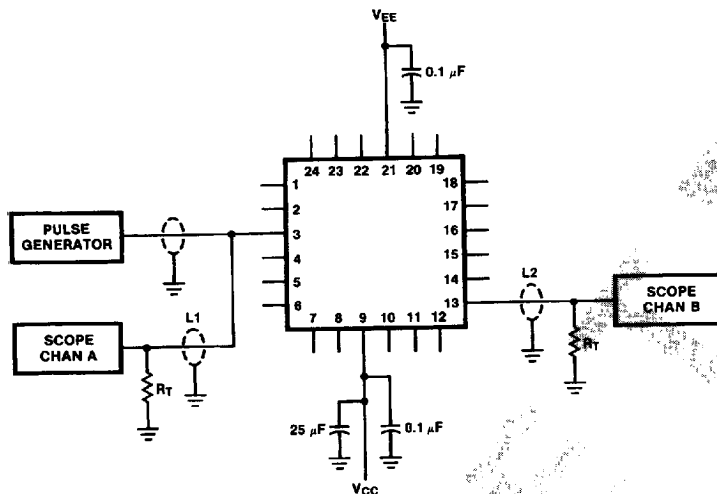


FIGURE 1. AC Test Circuit

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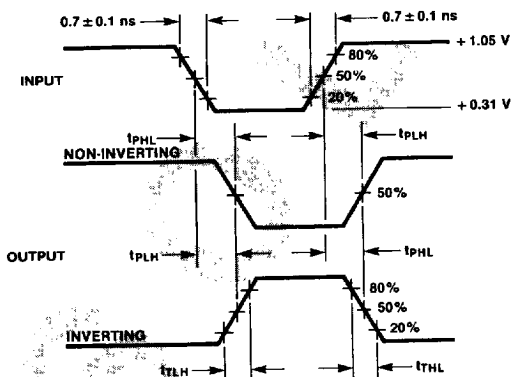


FIGURE 2. Propagation Delay and Transition Times

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Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- $L1$ and $L2$ = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol